PATENT ABSTRACTS OF JAPAN

(11)Publication number : 08-124300

(43)Date of publication of application : 17.05.1996

(51)Int.Cl. G11B 20/10

(21)Application number : 06-276346

(22)Date of filing : 10.11.1994

(71)Applicant : SANYO ELECTRIC CO LTD

(72)Inventor : NISHIKAWA MASAHIKO

last

(30)Priority

Priority number : 06 99937 Priority date : 13.05.1994 Priority country : JP

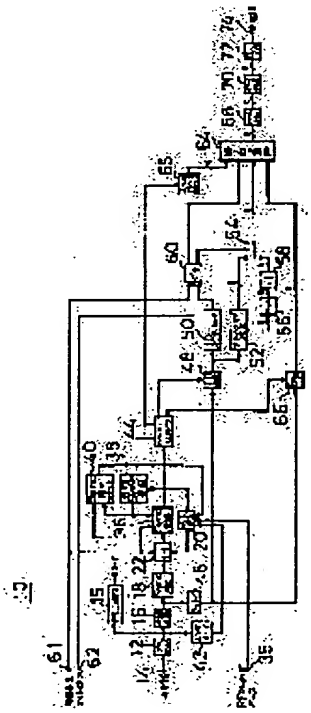
06207752 31.08.1994 JP

(54) MAGNETIC RECORDING AND REPRODUCING DEVICE

(57)Abstract:

PURPOSE: To excellently detect a synchronizing signal.

CONSTITUTION: A reproduced signal is amplified by a preamplifier 12 and demodulated by a demodulation circuit 16 and after that, a synchronizing signal is detected by a synchronizing signal detection circuit 18. A gate circuit 22 is operated by a gate signal generated by a gate signal generation circuit 20 for the synchronizing signal. A signal from the preamplifier 12 is inputted to an envelope detection circuit 42. When the result of the envelope detection is not more than a reference level, a gate is opened during the whole period of time and when the result is not less than the reference level, the gate is opened for a predetermined period of time. Thus, the gate operating period of time of the gate circuit 22 is switched over according to the result of the envelope detection.



LEGAL STATUS

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the digital signal magnetic recorder and reproducing device used for the digital video tape recorder which carries out record playback of the digital data, such as a digital video signal, especially, for example about a magnetic recorder and reproducing device.
[0002]
[Description of the Prior Art] About the noncommercial digital video tape recorder which carries out record playback of the digital data, such as a digital video signal, it is introduced to p.137 to p.150 of the Nikkei Business Publications issue and the Nikkei electronics book "a data compression and a data modulation", for example. Drawing 18 is the illustration Fig. which saw the magnetic tape from the field where the magnetic head contacts so that it may show the record format in this VTR, and the magnetic head is scanned toward a top from under a recording track.
[0003] Although four kinds of data are recorded on one truck, these data are the data for ** insertion and truck information, ** voice data, ** image data, and ** sub-code data at the order which the magnetic head scans. Such ten trucks (drawing 19 is the case of NTSC system and, in the case of PAL and SECAM, it becomes 12) gather like drawing 19 , and the image of one frame is formed. the block (drawing 19) with which it is said that image data are 135 sink blocks per each truck -- a truck 0 -- representing -- numbers 0, 1, --, 134 -- attaching -- the situation of the array of that block -- being shown -- although recorded, the detailed data format of this one block is shown in drawing 20 .
[0004] That is, ID signal (ID) which has information, such as that data parity (DATA PARITY), a synchronizing signal (SYNC), and a block number, and the parity signal (IDP) of this ID signal are added to the data (DATA) of an image, and each block is arranged like drawing 20 and formed. The signal of the 16-bit fixed pattern which consists of combination of 0 and 1 defined beforehand is recorded on this synchronizing signal, if the signal of this fixed pattern is detected at the time of playback, a synchronizing signal (detection synchronizing signal: refer to the drawing 2121) will be generated, and this will be used as a reference signal of signal processing. However, since the signal of this fixed pattern is the number of bits (2 bytes) of finite, the pattern signal same also in the bit string of data may appear, and this will be detected as an error synchronizing signal. Moreover, it originates in the blemish on a record medium etc., and a synchronizing signal may be missing.
[0005] Thus, in order to prevent incorrect detection and lack of a synchronizing signal, while creating an approach, i.e., a gate signal with the width of face of arbitration, as shown in drawing 21 from the former and covering a mask over periods other than the gate, when there is no synchronizing signal into the gate, the approach to which protection of a synchronization is applied with the protection synchronizing signal created by the counter is used. It explains with reference to the conventional magnetic recorder and reproducing device 1 which shows this actuation to drawing 22 .
[0006] After the regenerative signal inputted from input terminal 1a being amplified by pre amplifier 1b and getting over by demodulator 1c, the synchronizing signal pattern beforehand defined by 1d of synchronizing signal detectors is detected. In addition, a clock is generated by giving the output from pre amplifier 1b to PLL circuit 1b'. The gate is applied to the detected synchronizing signal at 1f of gate circuits by the gate signal

created by gate signal creation circuit 1e. As for gate signal creation circuit 1e, the gate is opened first in the first transition of RF switching pulse of a head, and 1f of gate circuits is in the condition that the gate has not started at the beginning. When a synchronizing signal is detected in this condition, using spacing of a synchronizing signal and a synchronizing signal being fixed, a gate signal will be created by gate signal creation circuit 1e with a counter (not shown), and the gate will be applied to the synchronizing signal detected from a degree. When the gate is applied to a synchronizing signal and a synchronizing signal does not exist within a gate period, protection is applied at 1g of synchronous protection networks by the protection synchronizing signal created in 1h of protection synchronizing signal creation circuits.

[0007] Moreover, if the condition that there is no synchronizing signal within a gate period continues and synchronous omission counted value (value which shows how many synchronizing signals fell out) turns into a certain defined value by synchronous omission count circuit 1i, the gate will once be opened, and if a synchronizing signal is detected, the gate will be closed again. Synchronous omission count circuit 1i is a circuit for preventing the error of a synchronizing signal spreading. Thus, the synchronizing signal with which protection was applied serves as criteria, and subsequent signal processing is performed with the output of pulse generator 1j which generates a synchronizing signal based on this.

[0008] On the other hand, after delay for the time amount which the signal outputted from demodulator circuit 1c needs for an above-mentioned synchronous digital disposal circuit delay-circuit 1k Goes out, based on the reference signal outputted from pulse generator 1j, ID signal is detected at 1l. of ID detectors. It is confirmed whether detected ID signal has an error in 1m of parity check circuits. On the other hand, detected ID signal is inputted into the other-end child of switch 1o through +1 adder 1q which adds "1" to latch circuit 1p and a sink block number while a sink block number is detected at 1n of block number detectors and it is inputted into one terminal of switch 1o. Switch 1o is controlled by the switch control signal outputted from gate circuit 1r, when the parity check of ID is O.K. (success) at the time of playback, it usually falls on the bottom, and it falls on the bottom at the time of NG (rejection).

[0009] That is, when the parity check of ID is O.K., the detected sink block number is inputted as a row address of the memory for error corrections of 1s of error correction circuits (not shown), and when the parity check of ID is NG, the value which added "1" to the sink number before 1 sink block is inputted as a row address of the memory for error corrections. Moreover, from column address counter 1t, the column address of the memory for error corrections is inputted. Furthermore, the write enable signal inputted from input terminal 1u is used as a write control signal of the memory for error corrections, after passing along gate circuit 1r.

[0010] Moreover, based on the signal outputted from pulse generator 1j, serial/parallel conversion of the signal with which delay was applied by delay circuit 1k is carried out by serial/parallel-conversion circuit 1v, and this data is written in on the address of the memory for error corrections detected previously. Thus, the data written in on the memory for error corrections per block are inputted into frame memory 1w, after an error correction is applied in 1s of error correction circuits and an error is corrected. In this frame memory 1w, the flag with which the data inputted from 1s of error correction circuits show whether it is the right is referred to, and data are written in for data only at the time of the right. That is, when the data of one frame ago will remain on frame memory 1w when data are wrong, therefore data are wrong, a signal can be interpolated by the data of one frame ago. Thus, since the interpolated data are compressed at the time of record, they are returned to the original data by data growth long-gyrus-of-insula way 1x, they are changed into an analog signal by D/A conversion circuit 1y, and are outputted from output terminal 1z.

[0011]

[Problem(s) to be Solved by the Invention] By the way, the truck shown in drawing 19 is recorded by the odd number truck and even number truck by the magnetic head from which an azimuth angle differs, respectively. That is, an odd number truck is recorded by the magnetic head of A azimuth, and an even number truck is recorded by the magnetic head of B azimuth.

[0012] Therefore, in order that the magnetic head may trace ranging over each truck at the time of special playback, while the magnetic head is tracing the truck of record of a reverse azimuth, an output level is small, and a synchronizing signal is not outputted at fixed spacing in many cases. For this reason, at the time of special playback, the gate is opened beforehand conventionally, and the technique of not applying protection, either is used. However, by this approach, since the gate is open also while the magnetic head is tracing the truck of the

same azimuth, possibility of considering that the mistaken synchronizing signal is a right synchronizing signal becomes large.

[0013] Moreover, although a mask is covered with a gate signal with the above-mentioned conventional technique in order to prevent detection of an error synchronizing signal, a blemish is on a record medium, or when a transit system is unstable, PLL circuit 1b' for clock generation malfunctions, and it shifts from the location originally outputted, and a synchronizing signal may be outputted. Although the synchronizing signal at this time is not an error synchronizing signal, if the width of face of an above-mentioned gate signal is too small, it may be undetectable, and if too conversely large, the probability to detect an error synchronizing signal will become large. Therefore, the engine performance of synchronizing signal detection is influenced by as how much the width of face of the gate is set.

[0014] Although gate width is based also on the engine performance of a transit system, if it is the transit system stabilized mostly, it is checked in the experiment that almost all synchronizing signals enter in **2 bits to the location of the synchronizing signal of normal. Therefore, it is common to set it as width of face of 5 bits as gate width. However, although the blemish on a record medium etc. is very rare owing to, it may not enter in **2 bits. For example, supposing the synchronizing signal is shifted more than the triplet to the location of normal, conventionally, this synchronizing signal will be disregarded and will be transposed to a protection synchronizing signal. Since subsequent processings are performed on the basis of this mistaken protection synchronizing signal, the data of this block will turn into mistaken data. And since the gate location to the following synchronizing signal was created on the basis of this mistaken protection synchronizing signal, this error had the trouble of being spread until only the count to which the synchronous omission was set continued and then the gate was opened.

[0015] Furthermore, at the time of special playback, while always moving switch 1o to the bottom by controlling gate circuit 1r by the special regenerative signal about the writing to the memory for error corrections in 1s of error correction circuits, when the result of the parity check of ID was NG, the mask of the write enable signal was carried out, the writing to memory was stopped, and the data of a front truck were used.

[0016] That is, at the time of special playback, the probability of a signal was judged based on the result of the parity check of ID, when the result of the parity check of ID was NG, it judged that an error was in the sink block number and data which were detected, the writing to the memory for error corrections in 1s of error correction circuits was stopped, only when the result of a parity check was O.K., it judged that it was right data and the writing to the memory for error corrections was performed.

[0017] To be sure, when the parity check of ID is O.K., it is confirmed by the experiment by the remarkable probability that data are right. However, it cannot generally crawl that an error is in a sink block number and data, and even if the result of a parity check is NG, a right case may also have a sink block number and data, just because the result of a parity check is NG. For example, the case where parts other than the sink block number of the ID signals are mistaken with the blemish of a record medium etc. is equivalent to this. Moreover, even if the part equivalent to the sink block number of the ID signals is mistaken, an error (1 bit and 2 bits) can be corrected by 1s of error correction circuits, and it cannot be said in this case that a sink block number and data are mistaken, either, just because the result of the parity check of ID is NG. Since such data were not stored in the memory for error corrections by the former in spite of it, there was a trouble that the amount of the right data stored in the memory for error corrections did not increase.

[0018] So, the main purpose of this invention is offering the magnetic recorder and reproducing device which can make detection precision of a synchronizing signal high. Moreover, other purposes of this invention are offering the magnetic recorder and reproducing device which can memorize more right data.

[0019]

[Means for Solving the Problem] The block including the data signal following the synchronizing signal and it which consists of digital signals, respectively is the magnetic recorder and reproducing device with which the truck which comes to be carried out two or more arrays plays the magnetic tape by which two or more formation was carried out to a magnetic tape, and the 1st invention is a magnetic recorder and reproducing device equipped with an adjustment means adjust the gate period of a gate circuit based on the synchronizing signal detector which detects a synchronizing signal from a regenerative signal, the gate circuit to which the synchronizing signal detected in the synchronizing signal detector is supplied, and the signal included in a

regenerative signal
[0020] The block including the synchronizing signal with which the 2nd invention consists of digital signals, respectively, ID signal which has the information on a block number, and the parity signal of ID is the magnetic recorder and reproducing device which plays the magnetic tape with which two or more formation of the truck which comes to carry out two or more arrays was carried out to a magnetic tape. ID detector which detects ID signal, the parity check circuit where detected ID signal judges whether it is the right, The block number detector which detects a sink block number from detected ID signal, It is a magnetic recorder and reproducing device equipped with the storage means for error corrections controlled whether ID signal writes in data according to the comparison result in the comparator which compares a right thing with a current sink block number, and a comparator among the sink block numbers detected before.
[0021]
[Function] In the 1st invention, the gate period of a gate circuit is adjusted by the adjustment means based on the signal included in a regenerative signal. For example, the level of a regenerative signal is detected in the level detector included in an adjustment means. As this level detector, an envelope detector circuit is used, for example. The gate width of a gate circuit is controlled based on this detection result. For example, if larger than the level defined beforehand, the 1st output is presented and the gate can open only the predetermined period corresponding to the appearance location of a synchronizing signal. On the other hand, if it is below the level defined beforehand, the 2nd output is presented and all the period gates can open.
[0022] Moreover, the 1st gate circuit and the 2nd gate circuit where gate periods differ as a gate circuit are prepared, a parity check and a block number are detected from ID signal, and either the 1st gate circuit and the 2nd gate circuit may be made to be chosen according to the result. At the time of O.K. of both of a parity check and the check of a block number, the 2nd long gate circuit of a gate period is chosen, and when that is not right, the 1st short gate circuit of a gate period is chosen. Thus, since the gate circuit where it differs within a gate period is chosen, although a synchronizing signal swings somewhat, a right synchronizing signal is detectable.
[0023] In the 2nd invention, it is judged for ID signal detected in ID detector in a parity check circuit whether it is the right. Only a right ID signal is inputted into a comparator. By the comparator, it is detected with a current sink block number before, and a right sink block number is compared for ID signal. Only when the current sink block number is larger, it is written in the storage means for error corrections, and data are not written in when that is not right.
[0024]
[Effect of the Invention] A synchronizing signal can be detected good, without considering that an error synchronizing signal is a right synchronizing signal unlike the former, since it has closed except the period when the gate can pass a desired synchronizing signal while according to this invention the gate is open while the magnetic head is tracing the truck of a reverse azimuth, for example at the time of the special playback at the time of 2X playback etc., and tracing the truck of the same azimuth. In addition, since protection of a synchronizing signal can be applied like the time of the usual playback at the time of special playback, a synchronizing signal can be detected still much more good.
[0025] Moreover, although almost all synchronizing signals go into **2 bits to the synchronizing signal location of normal, when ID signal detected on the basis of the synchronizing signal included in less than **2 bits is judged to be the right, the synchronizing signal can be trusted by the remarkable probability. Moreover, even if it is the synchronizing signal which is not contained in that the most is distributed around it, and less than **2 bits even if it is the synchronizing signal which does not go into less than **2 bits, when ID signal detected on the basis of the synchronizing signal is judged to be the right and other checks (check by the block number) other than the parity check of ID are set to O.K., the synchronizing signal can be trusted by the remarkable probability. Even if it does not enter in the **2-bit gate in view of such a point, it exists around the gate. And the ID signal is judged to be the right as a result of the parity check of ID detected by the synchronizing signal. In addition, when the check (check by the block number) by other approaches is set to O.K., [and] Since it is considered that the synchronizing signal is a right synchronizing signal, in the former, the synchronizing signal disregarded in spite of having been a right synchronizing signal can be detected as a right synchronizing signal, and a more reliable synchronizing signal can be detected.
[0026] Although the result of the parity check of ID is NG, since according to the 2nd invention the information

which does not have an error in a sink block number and data can be memorized correctly and more right data are obtained, a good special playback image can be obtained. The above-mentioned purpose of this invention, the other purposes, the description, and an advantage will become still clearer from the detailed explanation of the following examples given with reference to a drawing.

[0027]

[Example] Hereafter, although the example of this invention is explained, since the record format of a tape etc. is the same as that of drawing 18 - drawing 21 , that overlapping explanation is omitted. With reference to drawing 1 , the magnetic recorder and reproducing device 10 of this example contains pre amplifier 12. A regenerative signal is inputted into pre amplifier 12 from an input terminal 14, and it is amplified by pre amplifier 12, and after getting over in a demodulator circuit 16, the synchronizing signal pattern beforehand defined by the synchronizing signal detector 18 is detected. In addition, the output from pre amplifier 12 is given to the PLL circuit 15, and a clock is generated. The synchronizing signal detector 18 prevents detection of an error synchronizing signal. That concrete actuation gives the signal train of serial 0 obtained from pre amplifier 12, and 1 to the shift register in the synchronizing signal detector 18 (not shown), and the contents of this shift register are compared with the synchronizing signal detection pattern prepared beforehand. If they are in agreement, it will be regarded as a synchronizing signal and a synchronizing signal (detection synchronizing signal) will be generated. The gate is applied to this detected synchronizing signal by the gate signal created in the gate signal creation circuit 20 in a gate circuit 22.

[0028] The gate signal creation circuit 20 is constituted as shown in drawing 2 . Here, 1 sink block shown in drawing 20 is explained as 750 bits. The gate signal creation circuit 20 shown in drawing 2 contains the counter 23 for setting up the location which opens the gate. In a counter 23, if the protection synchronizing signal shown in drawing 3 (B) from the protection synchronizing signal creation circuit 38 (after-mentioned) is inputted, the count of the clock shown in drawing 3 (A) will be started (drawing 3 (D)), and the gate width setting circuit 24 containing a selector is connected to a counter 23, and the initial value in a counter 23 is set up by the gate width setting circuit 24. This gate width setting circuit 24 can set up gate width according to an envelope detector output. In this example, gate width when a high-level envelope detector output is given is made into 5 bits. That is, in order to make gate width into **2 bits, "2" is set up, and it is given to a counter 23. If the counted value of a counter 23 is set to "748", as shown in drawing 3 (D), a low level signal will be outputted from a decoder 26. This signal is given to JK-FF32 through an inverter 30 while it is given to a counter 28. Based on this signal, after 1 clock, JK-FF32 outputs the gate signal of a low level as shown in drawing 3 R> 3 (G), and opens the gate.

[0029] On the other hand, if the signal from a decoder 26 is inputted, a counter 28 will start the count of a clock (drawing 3 R> 3 (E)), and will give counted value as P to a comparator 34. "2" is given to a comparator 34 from the gate width setting circuit 24, and "4" which doubled this two is stored as criteria counted value Q. And if it becomes P=Q by the comparator 34, the pulse of a low level as shown in drawing 3 (F) will be given to JK-FF32. JK-FF32 outputs a high-level gate signal based on the standup of an after [1 clock of the signal (i.e., the signal)], and the gate is closed.

[0030] In addition, the gate opening pulse of a low level for always opening the gate is given to the PRE terminal of JK-FF32. While the gate opening pulse is given, the gate signal of a low level is outputted from JK-FF32, and the gate is always opened. As this gate opening pulse, the gate opening signal from others and RF switching pulse and the synchronous omission count circuit 40 (after-mentioned) is used. [output / of a low level / envelope detector]

[0031] To the gate circuit 22 which is in the condition that the gate has not started at the beginning, such a gate signal creation circuit 20 supplies the gate signal which opens the gate first in the first transition of RF switching pulse of the magnetic head which it is given from an input terminal 35 and shown in drawing 4 (A), and passes the detection synchronizing signal (drawing 4 (B)) which appears first. When a detection synchronizing signal is obtained in this condition, the counted value of a counter 23 will be counted by the gate signal creation circuit 24 using spacing of a synchronizing signal and a synchronizing signal being fixed (drawing 4 (C)), a gate signal will be created, and the gate like gate signal A shown in drawing 2 (D) will be applied to the synchronizing signal detected from a degree. When gate signal A is given to the gate circuit 22, from a gate circuit 22, the synchronizing signal A as shown in drawing 4 (E) is outputted.

[0032] Moreover, when the envelope detector signal of a low level is given to the gate signal creation circuit 20, gate signal B as shown in a gate circuit 22 at drawing 4 (F) is given, and from a gate circuit 22, the synchronizing signal B as shown in drawing 4 (G) is outputted at this time. It returns to drawing 1 and the synchronizing signal detected in the synchronizing signal detector 18 is given to a gate circuit 22. And the synchronizing signal detected within the gate period passes through a gate circuit 22 by opening a gate circuit 22 by the gate signal created in the gate signal creation circuit 20. While the mask of the error synchronizing signal generated on the other hand when the bit string same by chance as a synchronizing signal pattern was out of a gate period is carried out, when there is no synchronizing signal within a gate period, protection is applied in the synchronizing signal protection network 36 by the protection synchronizing signal created in the protection synchronizing signal creation circuit 38. If it puts in another way and a synchronizing signal will pass through a gate circuit 22, the synchronizing signal protection network 36 chooses and outputs the passed synchronizing signal and a synchronizing signal does not pass through a gate circuit 22, the synchronizing signal protection network 36 will choose and output the protection synchronizing signal obtained from the protection synchronizing signal creation circuit 38. In addition, a protection synchronizing signal is created by the counter in the protection synchronizing signal creation circuit 38 which makes a reset signal the output signal of the synchronizing signal protection network 36 (not shown).

[0033] Moreover, the condition that there is no synchronizing signal continues in the gate, and if synchronous omission counted value (value which shows how many times the synchronizing signal fell out) turns into a certain defined value in the synchronous omission count circuit 40, a gate opening signal will be given to the gate creation circuit 20. Then, if the gate is once altogether opened by the gate signal creation circuit 20 and a synchronizing signal is detected, the gate will be closed again. This is for preventing that the error of a synchronizing signal spreads.

[0034] Moreover, the signal amplified by pre amplifier 12 is the envelope detector circuit 42, the reference level set as arbitration is compared with the output level of an envelope, and the gate signal creation circuit 20 is controlled by the comparison result. Although an output level becomes small while the magnetic head is tracing the truck of a reverse azimuth at the time of special playback of the case below the reference level with which the envelope detector result was set as arbitration, i.e., 2X, 3X, etc., a gate circuit 22 is controlled to open the gate by gate signal B shown in drawing 4 (F). It acts so that all the synchronizing signals detected by this in the synchronizing signal detector 18 may regard it as a normal synchronizing signal. Thus, by opening the gate, a location gap of the synchronizing signal at the time of **** playback becomes a cause, and the situation where a synchronizing signal is no longer detected is avoided. That is, although an error synchronizing signal will also be incorporated, a required right synchronizing signal is surely detectable.

[0035] On the contrary, when the head is tracing the forward azimuth at the time of special playback, at the time of playback, an envelope detector result usually becomes larger than reference level, and gate signal A (drawing 4 (D)) is supplied to a gate circuit 22. When the synchronizing signal is not contained within the gate period at this time, it considers that the protection synchronizing signal created in the protection synchronizing signal creation circuit 38 is a normal synchronizing signal, and above-mentioned actuation of using it as a reference signal of subsequent signal processing is performed.

[0036] Thus, the synchronizing signal with which protection was applied serves as criteria, and subsequent signal processing is performed with the output of the pulse generator 44 which generates a reference signal based on this. From a pulse generator 44, the pulse for creating a pulse required in order to carry out serial/parallel conversion of the pulse for ID signal detection and the signal, and a column address is outputted.

[0037] On the other hand, after delay for the time amount which the signal outputted from a demodulator circuit 16 needs for an above-mentioned synchronous digital disposal circuit (18-40) is applied by the delay circuit 46, based on the reference signal outputted from a pulse generator 44, ID signal is detected in the ID detector 48. It is used as a row address of the memory for error corrections in the error correction circuit 64 which the block number contained in ID signal detected in this ID detector 48 mentions later (not shown).

[0038] That is, it is confirmed whether ID signal detected in the ID detector 48 has an error in the parity check circuit 50. On the other hand, detected ID signal is inputted into the other-end child of a switch 54 through a latch circuit 56 and +1 adder 58 which adds "1" to a sink block number while a sink block number is detected in the block number detector 52 and it is inputted into one terminal of a switch 54. A switch 54 is controlled by the

switch control signal outputted from a gate circuit 60.
[0039] Here, a gate circuit 60 is constituted as shown in drawing 5 . The gate circuit 60 shown in drawing 5 contains OR circuits 60a and 60b, NOR-circuit60c, and inverter 60d. ID parity check output (at the time of O.K. "high level") from the special regenerative signal (at the time of a special playback "high level") and the parity check circuit 50 from an input terminal 61 is inputted into OR circuit60a, and a switching control signal is outputted to it. Moreover, while a special regenerative signal is given through inverter 60d, ID parity check output is given to NOR-circuit60c. And with the output of NOR-circuit 60c, a write enable signal is inputted into OR circuit60b from an input terminal 62, and a write enable signal is outputted to it from OR circuit60b.
[0040] Therefore, at the time of playback, a switch 54 usually falls on the bottom, when the parity check of ID is O.K., and it falls on the bottom at the time of NG. At the time of the parity check [ID] O.K., the detected sink block number is inputted as a row address of the memory for error corrections in the error correction circuit 64, and when the parity check of ID is NG, the value which added "1" to the sink block number before 1 sink block is inputted as a row address of the memory for error corrections.
[0041] Moreover, the counted value of the column address counter 65 serves as a column address of the memory for error corrections in the error correction circuit 64. Here, the image Fig. of the memory for error corrections is shown in drawing 6 . Data are stored in video-data field 64a shown in drawing 6 . Moreover, after passing along a gate circuit 60, the write enable signal inputted from the input terminal 62 is used as a write control signal of the memory for error corrections in the error correction circuit 64, so that drawing 5 may show.

[0042] Moreover, by the signal outputted from a pulse generator 44, serial/parallel conversion of the signal with which delay was applied in the delay circuit 46 is carried out in the serial/parallel-conversion circuit 66, and it is written in as data on the address of the memory for error corrections in the error correction circuit 64. Thus, the data written in on the memory for error corrections per block are inputted into a frame memory 68, after an error correction is applied in the error correction circuit 64 and an error is corrected. In this frame memory 68, the flag with which the data inputted from the error correction circuit 64 show whether it is the right is referred to, and data are written in for data only at the time of the right. That is, when the data of one frame ago will remain on the frame memory 68 when data are mistaken, therefore data are wrong, a signal can be interpolated by the data of one frame ago. Thus, since the interpolated data are compressed at the time of record, they are returned to the original data on the data growth long-gyrus-of-insula way 70, they are changed into an analog signal by the D/A conversion circuit 72, and are outputted from an output terminal 74.
[0043] Actuation of such a magnetic recorder and reproducing device 10 is explained with reference to drawing 7 . First, if RF switching pulse is inputted in step S1, the gate will be opened in step S3. On the other hand, when step S1 is after "NO, i.e., RF switching pulse," is outputted, it progresses to step S5. In step S5, the gate signal of predetermined width of face is created in the gate signal creation circuit 20, and it progresses to step S7. In step S7, it is judged in the envelope detector circuit 42 whether it is envelope detector output > reference level. If step S7 is "NO", gate width will be changed in step S9. In this example, a gate signal which always opens the gate is created and gate width is changed. When step S7 is "YES", after processing of step S3 and S9, it progresses to step S11, respectively.
[0044] In step S11, detection of a synchronizing signal is performed in the synchronizing signal detector 18. Then, in step S13, if a synchronizing signal is detected, it will progress to step S15. In step S13, if the synchronizing signal is not detected, it progresses to step S17. In step S17, if the gate opening signal is outputted from the synchronous omission count circuit 40, the gate will be opened in step S19 and it will return to step S11.
[0045] On the other hand, if the gate opening signal is not outputted in step S17, in step S21, a protection synchronizing signal is created in the protection synchronizing signal creation circuit 38, and it progresses to step S15. At step S15, ID signal is detected in ID signal detector 48, and it progresses to step S23. In step S23, if the parity check of ID signal is right in the parity check circuit 50, in step S25, a sink block number is loaded to the memory for error corrections in the error correction circuit 64. On the other hand, if the parity check is mistaken in step S23, in step S27, "1" is added to the sink block number before 1 sink block, and the value is loaded to the memory for error corrections in step S29.
[0046] In addition, the control circuit 76 which controls gate width by the lock condition of PLL as shown in

drawing 8 instead of the envelope detector circuit 42 may be used. The control circuit 76 shown in drawing 8 includes the edge detector 78 where the edge of the data outputted from pre amplifier 12 is detected. The output from the edge detector 78 is given to AND circuit 82 through a monostable multivibrator 80. A clock is given to AND circuit 82 through an inverter 84, and the output of the AND gate 82 is given to a comparator 88 through a low pass filter 86. It is compared with a reference signal predetermined with a comparator 88, and the output according to the comparison result is given to the gate signal creation circuit 20.

[0047] Thus, in the control circuit 76 constituted, when PLL locks, the output from each circuit comes to be shown in drawing 9 (A), and the output of a comparator 88 serves as a low level. On the other hand, when PLL does not lock, the output from each circuit comes to be shown in drawing 9 (B), and the output of a comparator 88 becomes high-level. Subsequently, with reference to drawing 10 , the magnetic recorder and reproducing device 100 of other examples is explained. In addition, in a magnetic recorder and reproducing device 100, the overlapping explanation is omitted by attaching a same or similar reference number about the same component circuit as the magnetic recorder and reproducing device 10 shown in drawing 1 .

[0048] In this magnetic recorder and reproducing device 100, based on the synchronizing signal with which protection was applied, ID signal is detected by ID signal detector 48a from the signal acquired through a delay circuit 46, and a block number is detected by block number detector 52a. In addition, delay circuits 46 and 102a are formed here in order to double the timing of the signal inputted into ID signal detector 48a.

[0049] Although a parity check is performed by parity check circuit 50a, it is considered at this time that the block number detected when that result was O.K. is the right and that value becomes the row address of the memory for error corrections in the error correction circuit 64 as it is When it is NG, switch 54a is switched according to the signal from parity check circuit 50a so that the value which added "1" to the block number before 1 sink block latched by latch circuit 56a by +1 adder 58a may become the row address of the memory for error corrections.

[0050] On the other hand, the synchronizing signal (drawing 11 (A)) detected in the synchronizing signal detector 18 is also given to gate circuit 22b. With the gate signal of the width of face b (a<b) created by gate signal creation circuit 20b, the synchronizing signal detected within the gate period is passed by opening gate circuit 22b. The mask of the error synchronizing signal generated on the other hand when the bit string same by chance as a synchronizing signal pattern was out of a gate period is carried out.

[0051] Based on the synchronizing signal which passed this gate circuit 22b, ID signal is detected by ID signal detector 48b from the signal acquired through a delay circuit 46, and a block number is detected by block number detector 52b. And a parity check is performed by parity check circuit 50b, and ID signal is checked for no error.

[0052] Moreover, the block number detected from ID signal by block number detector 52b is given to a comparator circuit 104. Moreover, the value which the block number before 1 sink block outputted through switch 54b was latched by latch circuit 56b, and added "1" further by +1 adder 58b is given to a comparator 104. In a comparator 104, these two inputs are measured and it is judged for a block number whether it is the right.

[0053] Thus, in the processing relevant to the synchronizing signal which passed gate circuit 22b, while the parity check of ID signal is performed, the check of a block number is also performed, when these both are O.K., as for switches 54b and 106, the output from block number detector 52b is chosen, both the terminal of that bottom, i.e., switch 54b, and a switch 106 chooses the synchronizing signal outputted from gate circuit 22b. And when either is NG at least among the result of ID parity check in parity check circuit 50b, and the detection result in block number detector 52b when other namely, in switches 54b and 106, an upper terminal, i.e., switch 54b, chooses the output of switch 54a, respectively, and a switch 106 chooses the output of delay circuit 108a.

[0054] In addition, delay circuits 102b, 108a, and 108b are for adjusting the time lag which follows a circuit system on passing a signal. And it is used as a row address of the memory for error corrections in the error correction circuit 64, the output, i.e., the block number, of switch 54b, and the output of a switch 106 is inputted into a pulse generator 110, and the output from a pulse generator 110 is used as a reference signal of the serial/parallel-conversion machine 66 and the column address counter 65.

[0055] Thus, although it is stored in the memory for error corrections in the error correction circuit 64 after serial/parallel conversion of the signal outputted from the delay circuit 46 is carried out in the serial/parallel-

conversion circuit 66, at this time, the output of the column address counter 65 determines the column address of the memory for error corrections in the error correction circuit 64, and the block number outputted from switch 54b determines the row address of the memory for error corrections in the error correction circuit 64.
[0056] Such synchronizing signal detection actuation of a magnetic recorder and reproducing device 100 will become still clearer if drawing 11 is referred to. That is, drawing 11 (A) shows the output wave of the synchronizing signal detector 18, O in drawing shows a right synchronizing signal, and x shows an error synchronizing signal. That is, in this drawing, it is assumed that the 6th synchronizing signal (Sync6) is an error synchronizing signal.
[0057] Drawing 11 (B) shows the gate signal of width of face a, i.e., the output of gate signal creation circuit 20a, on the basis of the synchronizing signal with which it was applied, the output signal of the synchronizing signal protection network 36, i.e., the protection, shown in drawing 11 (E), within gate signal creation circuit 20a, a counter etc. is used for this gate signal and it is created. There is no gate signal of width of face a near a synchronizing signal (Sync5), because the counter in gate signal creation circuit 20a is reset by the synchronizing signal which the gate was opened by the gate opening signal (drawing 11 (D)) outputted from the synchronous omission count circuit 40, and was detected by this just before a gate signal was created. In addition, in this example, if the condition that there is no synchronizing signal continues twice in the gate signal of width of face a, gate circuit 22a will be opened compulsorily, and if the following synchronizing signal is detected in that condition, the case where the gate closes again is shown.
[0058] Here, the synchronizing signal (obtained from a protection synchronizing signal) which attached x although the synchronizing signal (Sync2) and synchronizing signal (Sync3) which are shown in drawing 11 are a right synchronizing signal, as a mask carried out with a gate signal, and detected as an error synchronizing signal, instead shown in drawing 11 (E) only in for example, gate circuit 22a will be detected accidentally.
[0059] Drawing 11 (C) shows the gate signal of gate width b, i.e., the output signal of gate circuit 22b, and comes to show the synchronizing signal to which the gate was applied by this gate signal in drawing 1111 (F). In this drawing 11 (F), since it is shown that the synchronizing signal which attached O is a right synchronizing signal, and the result of parity check circuit 50b serves as O.K., and the comparison result of a comparator circuit 104 is also in agreement, the switch 106 shown in drawing 10 switches to the bottom, and the synchronizing signal of drawing 11 R> 1 (F), i.e., drawing 11 , (J) is chosen.
[0060] On the other hand, since the synchronizing signal which attached x by drawing 11 (F) is an error synchronizing signal, as shown in drawing 11 (G), the result of parity check circuit 50b serves as NG (low level), and as shown in drawing 11 (H), the comparison result of a comparator circuit 104 serves as an inequality (low level). At this time, a switch 106 switches to the bottom and the synchronizing signal of drawing 11 (E) (I), i.e., drawing 9 , is outputted. Thus, the synchronizing signal outputted from a switch 106 comes to be shown in drawing 11 (K), and a right synchronizing signal without an error is detected.
[0061] Actuation of such a magnetic recorder and reproducing device is explained with reference to drawing 12 R> 2 and drawing 13 . As are shown in drawing 12 , and what gave "a" to the step number shows the processing about gate signal a and shows it to drawing 13 , what gave "b" to the step number shows the processing about gate signal b. Although these processings are performed by being parallel, processing of explanation concerning gate signal a first for convenience is explained previously.
[0062] First, in step S41a, if RS switching pulse is inputted, the gate of gate circuit 22a will be opened by gate signal creation circuit 20a in step S43a. On the other hand, after inputting "NO, i.e., RF switching pulse,", when step S41a is, Gate a is created by gate signal creation circuit 20a in step S45a. It progresses to step S47a after processing of step S43a and S45a.
[0063] In step S47a, detection of a synchronizing signal is performed by the synchronizing signal detector 18, and it progresses to step S49a by it. In step S49a, if a synchronizing signal is not detected, it progresses to step S51a. In step S51a, if the gate opening signal is outputted from the synchronous omission count circuit 40, the gate of gate circuit 22a will be opened in step S53a, and it will return to step S47a. In step S51a, if the gate opening signal is not outputted, in step S55a, a protection synchronizing signal is created by protection synchronizing signal creation circuit 26a. When a synchronizing signal is detected by step S49a, it progresses to step S57a after processing of S55a, and ID signal is detected by ID signal detector 48a, and it progresses to step S59a. In step S59a, if ID parity check by gate signal b is O.K., it will progress to step S61a. If the value and the

block number from block number detector 52b which added "1" to the sink block number before 1 sink block by gate signal b in step S61a are in agreement, it will connect with a lower terminal and switches 54b and 106 will progress to step S55b mentioned later.

[0064] When the time of step S59a being "NO" and step S61a are "NO(s)", it progresses to step S63a. In step S63a, if the parity check of ID signal is O.K. in parity check circuit 50a, in step S65a, a sink block number is loaded to the memory for error corrections in the error correction circuit 64. On the other hand, if step S63a is "NO", in step S67a, "1" is added to the block number in front of 1 synchronizing signal, and the value is stored in the memory for error corrections in step S69a.

[0065] On the other hand, in step S41b shown in drawing 13 , if RF switching pulse is given, the gate of gate circuit 22b will be opened in step S43b. If step S41b is "NO", in step S45b, gate signal b will be created by gate signal creation circuit 20b, and it will be given to gate circuit 22b. It progresses to step S47b after processing of step S43b and S45b.

[0066] In step S47b, if the gate opening signal by gate signal a is outputted, it will progress to step S49b. In step S49b, the gate of gate circuit 22b is opened and it progresses to step S51b. Also when step S47b is "NO", it progresses to step S51b. In step S51b, detection of a synchronizing signal is performed in the synchronizing signal detector 18, ID signal is detected by ID detector 48b in step S53b, and it progresses to step S55b.

[0067] In step S55b, if ID parity check in parity check circuit 50b is O.K., in step S57b, a sink block number will be detected by block number detector 52b, and it will progress to step S59b. In step S59b, if the value and the block number from block number detector 52b which added "1" to the block number before 1 sink block are in agreement, the sink block number is stored in the memory for error corrections in the error correction circuit 64 in step S61b.

[0068] When the time of step S55b being "NO" and step S59b are "NO(s)", it progresses to step S59a. In addition, step S61a is "YES", and when progressing to step S55b, naturally step S55b and S59b are set to "YES." Moreover, since step S55b and S59b are "NO(s)", when progressing to step S59a, naturally step S59a is set to "NO."

[0069] Furthermore, with reference to drawing 14 , the magnetic recorder and reproducing device 120 of other examples is explained. In addition, it becomes being the same as that of the magnetic recorder and reproducing device 10 which also shows circuit actuation to drawing 1 since it is fundamentally constituted similarly although gate width of the gate signal created in the gate signal creation circuit 20, corresponding to the detection result of the envelope detector circuit 42 like the magnetic recorder and reproducing device 10 which shows a magnetic recorder and reproducing device 120 to drawing 1 is not changed, and a switch 54 is usually controlled by the output of the parity check circuit 50 at the time of playback and mask actuation of a mask 122 is canceled. Therefore, the explanation which overlaps by attaching the same number is omitted.

[0070] Therefore, below, the main points which should be noted are explained among the actuation about the time of special playback. The sink block number outputted from a switch 54 is inputted into a comparator 124 and a latch circuit 126. The output of a latch circuit 126 is reset in the first transition of RF switching pulse, and the value has become "0" at the beginning. And the output of the parity check circuit 50 of ID signal is seen, and only when a parity check is O.K., the sink block number which is the output of a switch 54 is latched by the latch circuit 126.

[0071] That is, the output of a latch circuit 126 is updated only when the parity check of ID is O.K., and that whose parity check of ID is O.K. among sink block numbers smaller than the present sink block number is always outputted. This value is compared with a current sink block number, the write enable mask signal of a low level is outputted for a current sink block number from a comparator 124 at the time of below the sink block number from a latch circuit 126, the mask of the write enable signal is carried out in the mask circuit 122, and the writing to the memory for error corrections in the error correction circuit 64 is stopped by the comparator 124. On the other hand, when the current sink block number is larger, a high-level write enable mask signal is outputted from a comparator 124, and data are written in on the address created with the sink block number and the KARAMO address counter 65.

[0072] Here, the mask circuit 122 is constituted as shown in drawing 1515 . The mask circuit 122 shown in drawing 2 contains OR circuit 128, the NOR gate 130, and an inverter 132. While the signal from an input terminal 61 is given to NOR circuit 130 through an inverter 132, the write enable mask signal from a

comparator circuit 124 is given. The write enable signal from the output and input terminal 62 of NOR circuit 130 is given to OR circuit 128, and the output of OR circuit 128 is given to the error correction circuit 64 as an output of the mask circuit 122.

[0073] In the mask circuit 122, if the special regenerative signal and the write enable mask signal of a low level are outputted, a write enable signal will not be outputted to the error correction circuit 64. On the other hand, when the high-level write enable mask signal is outputted, a write enable signal is given to the error correction circuit 64. If it explains with reference to drawing 16 , from the synchronizing signal protection network 36, a protection synchronizing signal as shown in drawing 16 (A) will be outputted, and ID detection pulse as shown in drawing 16 (B) will be outputted from a pulse generator 44 according to it. And from the parity check circuit 50, a signal as shown in drawing 16 (C) is outputted. Since the protection synchronizing signal (Sync2) shown in drawing 16 (A) is mistaken, according to it, the output from the parity check circuit 50 is set to a low level.

[0074] As the sink block number outputted through a switch 54 shows drawing 16 (D) at this time, when the case where it is set to "30->25->32->33->34" is assumed, "25" is the mistaken sink block number. According to it, the sink block number from a latch circuit 126 is set to "29->30->30->32->33." "30" which the latch circuit 126 did not hold the mistaken sink block number "25", but incorporated it before that is held as it is so that drawing 16 (D) and (E) may be compared and understood. And a comparator 124 compares two signals inputted, and in below the sink block number from the latch circuit 126 which the present sink block number shown in drawing 16 (D) shows to drawing 16 (E), as shown in drawing 16 (F), a comparator 124 outputs the write enable mask signal of a low level in the mask circuit 122. Then, from OR circuit 128 of the mask circuit 122, a write enable signal is not outputted but the writing of the data to the memory for error corrections in the error correction circuit 64 is stopped.

[0075] Main actuation of such a magnetic recorder and reproducing device 120 is explained with reference to drawing 17 . First, in step S71 shown in drawing 17 , if RF switching pulse is given, it will progress to step S73. The gate of a gate circuit 22 is opened in step S73. On the other hand, if step S71 is "NO", in step S75, the gate signal of predetermined width of face will be created, and the gate will be set up. After processing of steps S73 and S75 progresses to step S77, respectively. In step S77, if detection of a synchronizing signal is performed and a synchronizing signal is not detected in step S79 in the synchronizing signal detector 18, it progresses to step S81. In step S81, if the gate opening signal is outputted from the synchronous omission count circuit 40, the gate of a gate circuit 22 will be opened in step S83, and it will return to step S77. On the other hand, if the gate opening signal is not outputted in step S81, in step S85, a protection synchronizing signal is created in the protection synchronizing signal creation circuit 38, and it progresses to step S87. Also when step S79 is "NO", it progresses to step S87.

[0076] In step S87, ID signal is detected in the ID detector 48, and if ID parity check is O.K. in step S89a in the parity check circuit 50, in step S91a, a sink block number will be latched by the latch circuit 126, and it will progress to step S93. It progresses to the direct step S93, without updating a sink block number, if the parity check of ID signal is NG in step S89a. Moreover, in after [processing] step S89b of step S87, a sink block number current in the block number detector 52 is detected, and it progresses to step S93.

[0077] In step S93, a sink block number current by the comparator 124 is compared with the sink block number from a latch circuit 126. If the current sink block number is larger, in step S95, a current sink block number will be written in the memory for error corrections in the error correction circuit 64. In step S93, if a current sink block number is below a sink block number from a latch circuit 126, in step S97, the writing of the data to the memory for error corrections in the error correction circuit 64 will be stopped.

[0078] In addition, although the above-mentioned example explained the magnetic recorder and reproducing device which records digital data on a magnetic tape, it cannot be overemphasized that this invention is applicable also to the record regenerative apparatus of an optical recording method.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] A synchronizing signal can be detected good, without considering that an error synchronizing signal is a right synchronizing signal unlike the former, since it has closed except the period when the gate can pass a desired synchronizing signal while according to this invention the gate is open while the magnetic head is tracing the truck of a reverse azimuth, for example at the time of the special playback at the time of 2X playback etc., and tracing the truck of the same azimuth. In addition, since protection of a synchronizing signal can be applied like the time of the usual playback at the time of special playback, a synchronizing signal can be detected still much more good.

[0025] Moreover, although almost all synchronizing signals go into **2 bits to the synchronizing signal location of normal, when ID signal detected on the basis of the synchronizing signal included in less than **2 bits is judged to be the right, the synchronizing signal can be trusted by the remarkable probability. Moreover, even if it is the synchronizing signal which is not contained in that the most is distributed around it, and less than **2 bits even if it is the synchronizing signal which does not go into less than **2 bits, when ID signal detected on the basis of the synchronizing signal is judged to be the right and other checks (check by the block number) other than the parity check of ID are set to O.K., the synchronizing signal can be trusted by the remarkable probability. Even if it does not enter in the **2-bit gate in view of such a point, it exists around the gate. And the ID signal is judged to be the right as a result of the parity check of ID detected by the synchronizing signal. In addition, when the check (check by the block number) by other approaches is set to O.K., [and] Since it is considered that the synchronizing signal is a right synchronizing signal, in the former, the synchronizing signal disregarded in spite of having been a right synchronizing signal can be detected as a right synchronizing signal, and a more reliable synchronizing signal can be detected.

[0026] Although the result of the parity check of ID is NG, since according to the 2nd invention the information which does not have an error in a sink block number and data can be memorized correctly and more right data are obtained, a good special playback image can be obtained. The above-mentioned purpose of this invention, the other purposes, the description, and an advantage will become still clearer from the detailed explanation of the following examples given with reference to a drawing.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By the way, the truck shown in drawing 19 is recorded by the odd number truck and even number truck by the magnetic head from which an azimuth angle differs, respectively. That is, an odd number truck is recorded by the magnetic head of A azimuth, and an even number truck is recorded by the magnetic head of B azimuth.

[0012] Therefore, in order that the magnetic head may trace ranging over each truck at the time of special playback, while the magnetic head is tracing the truck of record of a reverse azimuth, an output level is small, and a synchronizing signal is not outputted at fixed spacing in many cases. For this reason, at the time of special playback, the gate is opened beforehand conventionally, and the technique of not applying protection, either is used. However, by this approach, since the gate is open also while the magnetic head is tracing the truck of the same azimuth, possibility of considering that the mistaken synchronizing signal is a right synchronizing signal becomes large.

[0013] Moreover, although a mask is covered with a gate signal with the above-mentioned conventional technique in order to prevent detection of an error synchronizing signal, a blemish is on a record medium, or when a transit system is unstable, PLL circuit 1b' for clock generation malfunctions, and it shifts from the location originally outputted, and a synchronizing signal may be outputted. Although the synchronizing signal at this time is not an error synchronizing signal, if the width of face of an above-mentioned gate signal is too small, it may be undetectable, and if too conversely large, the probability to detect an error synchronizing signal will become large. Therefore, the engine performance of synchronizing signal detection is influenced by as how much the width of face of the gate is set.

[0014] Although gate width is based also on the engine performance of a transit system, if it is the transit system stabilized mostly, it is checked in the experiment that almost all synchronizing signals enter in **2 bits to the location of the synchronizing signal of normal. Therefore, it is common to set it as width of face of 5 bits as gate width. However, although the blemish on a record medium etc. is very rare owing to, it may not enter in **2 bits. For example, supposing the synchronizing signal is shifted more than the triplet to the location of normal, conventionally, this synchronizing signal will be disregarded and will be transposed to a protection synchronizing signal. Since subsequent processings are performed on the basis of this mistaken protection synchronizing signal, the data of this block will turn into mistaken data. And since the gate location to the following synchronizing signal was created on the basis of this mistaken protection synchronizing signal, this error had the trouble of being spread until only the count to which the synchronous omission was set continued and then the gate was opened.

[0015] Furthermore, at the time of special playback, while always moving switch 1o to the bottom by controlling gate circuit 1r by the special regenerative signal about the writing to the memory for error corrections in 1s of error correction circuits, when the result of the parity check of ID was NG, the mask of the write enable signal was carried out, the writing to memory was stopped, and the data of a front truck were used.

[0016] That is, at the time of special playback, the probability of a signal was judged based on the result of the parity check of ID, when the result of the parity check of ID was NG, it judged that an error was in the sink block number and data which were detected, the writing to the memory for error corrections in 1s of error correction circuits was stopped, only when the result of a parity check was O.K., it judged that it was right data and the writing to the memory for error corrections was performed.

[0017] To be sure, when the parity check of ID is O.K., it is confirmed by the experiment by the remarkable probability that data are right. However, it cannot generally crawl that an error is in a sink block number and data, and even if the result of a parity check is NG, a right case may also have a sink block number and data, just because the result of a parity check is NG. For example, the case where parts other than the sink block number of the ID signals are mistaken with the blemish of a record medium etc. is equivalent to this. Moreover, even if the part equivalent to the sink block number of the ID signals is mistaken, an error (1 bit and 2 bits) can be corrected by 1s of error correction circuits, and it cannot be said in this case that a sink block number and data are mistaken, either, just because the result of the parity check of ID is NG. Since such data were not stored in the memory for error corrections by the former in spite of it, there was a trouble that the amount of the right data stored in the memory for error corrections did not increase.

[0018] So, the main purpose of this invention is offering the magnetic recorder and reproducing device which can make detection precision of a synchronizing signal high. Moreover, other purposes of this invention are offering the magnetic recorder and reproducing device which can memorize more right data.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

OPERATION

[Function] In the 1st invention, the gate period of a gate circuit is adjusted by the adjustment means based on the signal included in a regenerative signal. For example, the level of a regenerative signal is detected in the level detector included in an adjustment means. As this level detector, an envelope detector circuit is used, for example. The gate width of a gate circuit is controlled based on this detection result. For example, if larger than the level defined beforehand, the 1st output is presented and the gate can open only the predetermined period corresponding to the appearance location of a synchronizing signal. On the other hand, if it is below the level defined beforehand, the 2nd output is presented and all the period gates can open.
[0022] Moreover, the 1st gate circuit and the 2nd gate circuit where gate periods differ as a gate circuit are prepared, a parity check and a block number are detected from ID signal, and either the 1st gate circuit and the 2nd gate circuit may be made to be chosen according to the result. At the time of O.K. of both of a parity check and the check of a block number, the 2nd long gate circuit of a gate period is chosen, and when that is not right, the 1st short gate circuit of a gate period is chosen. Thus, since the gate circuit where it differs within a gate period is chosen, although a synchronizing signal swings somewhat, a right synchronizing signal is detectable.
[0023] In the 2nd invention, it is judged for ID signal detected in ID detector in a parity check circuit whether it is the right. Only a right ID signal is inputted into a comparator. By the comparator, it is detected with a current sink block number before, and a right sink block number is compared for ID signal. Only when the current sink block number is larger, it is written in the storage means for error corrections, and data are not written in when that is not right.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EXAMPLE

[Example] Hereafter, although the example of this invention is explained, since the record format of a tape etc. is the same as that of drawing 18 - drawing 21 , that overlapping explanation is omitted. With reference to drawing 1 , the magnetic recorder and reproducing device 10 of this example contains pre amplifier 12. A regenerative signal is inputted into pre amplifier 12 from an input terminal 14, and it is amplified by pre amplifier 12, and after getting over in a demodulator circuit 16, the synchronizing signal pattern beforehand defined by the synchronizing signal detector 18 is detected. In addition, the output from pre amplifier 12 is given to the PLL circuit 15, and a clock is generated. The synchronizing signal detector 18 prevents detection of an error synchronizing signal. That concrete actuation gives the signal train of serial 0 obtained from pre amplifier 12, and 1 to the shift register in the synchronizing signal detector 18 (not shown), and the contents of this shift register are compared with the synchronizing signal detection pattern prepared beforehand. If they are in agreement, it will be regarded as a synchronizing signal and a synchronizing signal (detection synchronizing signal) will be generated. The gate is applied to this detected synchronizing signal by the gate signal created in the gate signal creation circuit 20 in a gate circuit 22.
[0028] The gate signal creation circuit 20 is constituted as shown in drawing 2 . Here, 1 sink block shown in drawing 20 is explained as 750 bits. The gate signal creation circuit 20 shown in drawing 2 contains the counter 23 for setting up the location which opens the gate. In a counter 23, if the protection synchronizing signal shown in drawing 3 (B) from the protection synchronizing signal creation circuit 38 (after-mentioned) is inputted, the count of the clock shown in drawing 3 (A) will be started (drawing 3 (D)), and the gate width setting circuit 24 containing a selector is connected to a counter 23, and the initial value in a counter 23 is set up by the gate width setting circuit 24. This gate width setting circuit 24 can set up gate width according to an envelope detector output. In this example, gate width when a high-level envelope detector output is given is made into 5 bits. That is, in order to make gate width into **2 bits, "2" is set up, and it is given to a counter 23. If the counted value of a counter 23 is set to "748", as shown in drawing 3 (D), a low level signal will be outputted from a decoder 26. This signal is given to JK-FF32 through an inverter 30 while it is given to a counter 28. Based on this signal, after 1 clock, JK-FF32 outputs the gate signal of a low level as shown in drawing 3 R> 3 (G), and opens the gate.
[0029] On the other hand, if the signal from a decoder 26 is inputted, a counter 28 will start the count of a clock (drawing 3 R> 3 (E)), and will give counted value as P to a comparator 34. "2" is given to a comparator 34 from the gate width setting circuit 24, and "4" which doubled this two is stored as criteria counted value Q. And if it becomes P=Q by the comparator 34, the pulse of a low level as shown in drawing 3 (F) will be given to JK-FF32. JK-FF32 outputs a high-level gate signal based on the standup of an after [1 clock of the signal (i.e., the signal)], and the gate is closed.
[0030] In addition, the gate opening pulse of a low level for always opening the gate is given to the PRE terminal of JK-FF32. While the gate opening pulse is given, the gate signal of a low level is outputted from JK-FF32, and the gate is always opened. As this gate opening pulse, the gate opening signal from others and RF switching pulse and the synchronous omission count circuit 40 (after-mentioned) is used. [output / of a low level / envelope detector]
[0031] To the gate circuit 22 which is in the condition that the gate has not started at the beginning, such a gate signal creation circuit 20 supplies the gate signal which opens the gate first in the first transition of RF

switching pulse of the magnetic head which it is given from an input terminal 35 and shown in drawing 4 (A), and passes the detection synchronizing signal (drawing 4 (B)) which appears first. When a detection synchronizing signal is obtained in this condition, the counted value of a counter 23 will be counted by the gate signal creation circuit 24 using spacing of a synchronizing signal and a synchronizing signal being fixed (drawing 4 (C)), a gate signal will be created, and the gate like gate signal A shown in drawing 2 (D) will be applied to the synchronizing signal detected from a degree. When gate signal A is given to the gate circuit 22, from a gate circuit 22, the synchronizing signal A as shown in drawing 4 (E) is outputted.

[0032] Moreover, when the envelope detector signal of a low level is given to the gate signal creation circuit 20, gate signal B as shown in a gate circuit 22 at drawing 4 (F) is given, and from a gate circuit 22, the synchronizing signal B as shown in drawing 4 (G) is outputted at this time. It returns to drawing 1 and the synchronizing signal detected in the synchronizing signal detector 18 is given to a gate circuit 22. And the synchronizing signal detected within the gate period passes through a gate circuit 22 by opening a gate circuit 22 by the gate signal created in the gate signal creation circuit 20. While the mask of the error synchronizing signal generated on the other hand when the bit string same by chance as a synchronizing signal pattern was out of a gate period is carried out, when there is no synchronizing signal within a gate period, protection is applied in the synchronizing signal protection network 36 by the protection synchronizing signal created in the protection synchronizing signal creation circuit 38. If it puts in another way and a synchronizing signal will pass through a gate circuit 22, the synchronizing signal protection network 36 chooses and outputs the passed synchronizing signal and a synchronizing signal does not pass through a gate circuit 22, the synchronizing signal protection network 36 will choose and output the protection synchronizing signal obtained from the protection synchronizing signal creation circuit 38. In addition, a protection synchronizing signal is created by the counter in the protection synchronizing signal creation circuit 38 which makes a reset signal the output signal of the synchronizing signal protection network 36 (not shown).

[0033] Moreover, the condition that there is no synchronizing signal continues in the gate, and if synchronous omission counted value (value which shows how many times the synchronizing signal fell out) turns into a certain defined value in the synchronous omission count circuit 40, a gate opening signal will be given to the gate creation circuit 20. Then, if the gate is once altogether opened by the gate signal creation circuit 20 and a synchronizing signal is detected, the gate will be closed again. This is for preventing that the error of a synchronizing signal spreads.

[0034] Moreover, the signal amplified by pre amplifier 12 is the envelope detector circuit 42, the reference level set as arbitration is compared with the output level of an envelope, and the gate signal creation circuit 20 is controlled by the comparison result. Although an output level becomes small while the magnetic head is tracing the truck of a reverse azimuth at the time of special playback of the case below the reference level with which the envelope detector result was set as arbitration, i.e., 2X, 3X, etc., a gate circuit 22 is controlled to open the gate by gate signal B shown in drawing 4 (F). It acts so that all the synchronizing signals detected by this in the synchronizing signal detector 18 may regard it as a normal synchronizing signal. Thus, by opening the gate, a location gap of the synchronizing signal at the time of **** playback becomes a cause, and the situation where a synchronizing signal is no longer detected is avoided. That is, although an error synchronizing signal will also be incorporated, a required right synchronizing signal is surely detectable.

[0035] On the contrary, when the head is tracing the forward azimuth at the time of special playback, at the time of playback, an envelope detector result usually becomes larger than reference level, and gate signal A (drawing 4 (D)) is supplied to a gate circuit 22. When the synchronizing signal is not contained within the gate period at this time, it considers that the protection synchronizing signal created in the protection synchronizing signal creation circuit 38 is a normal synchronizing signal, and above-mentioned actuation of using it as a reference signal of subsequent signal processing is performed.

[0036] Thus, the synchronizing signal with which protection was applied serves as criteria, and subsequent signal processing is performed with the output of the pulse generator 44 which generates a reference signal based on this. From a pulse generator 44, the pulse for creating a pulse required in order to carry out serial/parallel conversion of the pulse for ID signal detection and the signal, and a column address is outputted.

[0037] On the other hand, after delay for the time amount which the signal outputted from a demodulator circuit 16 needs for an above-mentioned synchronous digital disposal circuit (18-40) is applied by the delay circuit 46,

based on the reference signal outputted from a pulse generator 44, ID signal is detected in the ID detector 48. It is used as a row address of the memory for error corrections in the error correction circuit 64 which the block number contained in ID signal detected in this ID detector 48 mentions later (not shown).
[0038] That is, it is confirmed whether ID signal detected in the ID detector 48 has an error in the parity check circuit 50. On the other hand, detected ID signal is inputted into the other-end child of a switch 54 through a latch circuit 56 and +1 adder 58 which adds "1" to a sink block number while a sink block number is detected in the block number detector 52 and it is inputted into one terminal of a switch 54. A switch 54 is controlled by the switch control signal outputted from a gate circuit 60.
[0039] Here, a gate circuit 60 is constituted as shown in drawing 5 . The gate circuit 60 shown in drawing 5 contains OR circuits 60a and 60b, NOR-circuit60c, and inverter 60d. ID parity check output (at the time of O.K. "high level") from the special regenerative signal (at the time of a special playback "high level") and the parity check circuit 50 from an input terminal 61 is inputted into OR circuit60a, and a switching control signal is outputted to it. Moreover, while a special regenerative signal is given through inverter 60d, ID parity check output is given to NOR-circuit60c. And with the output of NOR-circuit 60c, a write enable signal is inputted into OR circuit60b from an input terminal 62, and a write enable signal is outputted to it from OR circuit60b.
[0040] Therefore, at the time of playback, a switch 54 usually falls on the bottom, when the parity check of ID is O.K., and it falls on the bottom at the time of NG. At the time of the parity check [ID] O.K., the detected sink block number is inputted as a row address of the memory for error corrections in the error correction circuit 64, and when the parity check of ID is NG, the value which added "1" to the sink block number before 1 sink block is inputted as a row address of the memory for error corrections.
[0041] Moreover, the counted value of the column address counter 65 serves as a column address of the memory for error corrections in the error correction circuit 64. Here, the image Fig. of the memory for error corrections is shown in drawing 6 . Data are stored in video-data field 64a shown in drawing 6 . Moreover, after passing along a gate circuit 60, the write enable signal inputted from the input terminal 62 is used as a write control signal of the memory for error corrections in the error correction circuit 64, so that drawing 5 may show.

[0042] Moreover, by the signal outputted from a pulse generator 44, serial/parallel conversion of the signal with which delay was applied in the delay circuit 46 is carried out in the serial/parallel-conversion circuit 66, and it is written in as data on the address of the memory for error corrections in the error correction circuit 64. Thus, the data written in on the memory for error corrections per block are inputted into a frame memory 68, after an error correction is applied in the error correction circuit 64 and an error is corrected. In this frame memory 68, the flag with which the data inputted from the error correction circuit 64 show whether it is the right is referred to, and data are written in for data only at the time of the right. That is, when the data of one frame ago will remain on the frame memory 68 when data are mistaken, therefore data are wrong, a signal can be interpolated by the data of one frame ago. Thus, since the interpolated data are compressed at the time of record, they are returned to the original data on the data growth long-gyrus-of-insula way 70, they are changed into an analog signal by the D/A conversion circuit 72, and are outputted from an output terminal 74.
[0043] Actuation of such a magnetic recorder and reproducing device 10 is explained with reference to drawing 7 . First, if RF switching pulse is inputted in step S1, the gate will be opened in step S3. On the other hand, when step S1 is after "NO, i.e., RF switching pulse," is outputted, it progresses to step S5. In step S5, the gate signal of predetermined width of face is created in the gate signal creation circuit 20, and it progresses to step S7. In step S7, it is judged in the envelope detector circuit 42 whether it is envelope detector output > reference level. If step S7 is "NO", gate width will be changed in step S9. In this example, a gate signal which always opens the gate is created and gate width is changed. When step S7 is "YES", after processing of step S3 and S9, it progresses to step S11, respectively.
[0044] In step S11, detection of a synchronizing signal is performed in the synchronizing signal detector 18. Then, in step S13, if a synchronizing signal is detected, it will progress to step S15. In step S13, if the synchronizing signal is not detected, it progresses to step S17. In step S17, if the gate opening signal is outputted from the synchronous omission count circuit 40, the gate will be opened in step S19 and it will return to step S11.
[0045] On the other hand, if the gate opening signal is not outputted in step S17, in step S21, a protection

synchronizing signal is created in the protection synchronizing signal creation circuit 38, and it progresses to step S15. At step S15, ID signal is detected in ID signal detector 48, and it progresses to step S23. In step S23, if the parity check of ID signal is right in the parity check circuit 50, in step S25, a sink block number is loaded to the memory for error corrections in the error correction circuit 64. On the other hand, if the parity check is mistaken in step S23, in step S27, "1" is added to the sink block number before 1 sink block, and the value is loaded to the memory for error corrections in step S29.

[0046] In addition, the control circuit 76 which controls gate width by the lock condition of PLL as shown in drawing 8 instead of the envelope detector circuit 42 may be used. The control circuit 76 shown in drawing 8 includes the edge detector 78 where the edge of the data outputted from pre amplifier 12 is detected. The output from the edge detector 78 is given to AND circuit 82 through a monostable multivibrator 80. A clock is given to AND circuit 82 through an inverter 84, and the output of the AND gate 82 is given to a comparator 88 through a low pass filter 86. It is compared with a reference signal predetermined with a comparator 88, and the output according to the comparison result is given to the gate signal creation circuit 20.

[0047] Thus, in the control circuit 76 constituted, when PLL locks, the output from each circuit comes to be shown in drawing 9 (A), and the output of a comparator 88 serves as a low level. On the other hand, when PLL does not lock, the output from each circuit comes to be shown in drawing 9 (B), and the output of a comparator 88 becomes high-level. Subsequently, with reference to drawing 10 , the magnetic recorder and reproducing device 100 of other examples is explained. In addition, in a magnetic recorder and reproducing device 100, the overlapping explanation is omitted by attaching a same or similar reference number about the same component circuit as the magnetic recorder and reproducing device 10 shown in drawing 1 .

[0048] In this magnetic recorder and reproducing device 100, based on the synchronizing signal with which protection was applied, ID signal is detected by ID signal detector 48a from the signal acquired through a delay circuit 46, and a block number is detected by block number detector 52a. In addition, delay circuits 46 and 102a are formed here in order to double the timing of the signal inputted into ID signal detector 48a.

[0049] Although a parity check is performed by parity check circuit 50a, it is considered at this time that the block number detected when that result was O.K. is the right and that value becomes the row address of the memory for error corrections in the error correction circuit 64 as it is When it is NG, switch 54a is switched according to the signal from parity check circuit 50a so that the value which added "1" to the block number before 1 sink block latched by latch circuit 56a by +1 adder 58a may become the row address of the memory for error corrections.

[0050] On the other hand, the synchronizing signal (drawing 11 (A)) detected in the synchronizing signal detector 18 is also given to gate circuit 22b. With the gate signal of the width of face b (a<b) created by gate signal creation circuit 20b, the synchronizing signal detected within the gate period is passed by opening gate circuit 22b. The mask of the error synchronizing signal generated on the other hand when the bit string same by chance as a synchronizing signal pattern was out of a gate period is carried out.

[0051] Based on the synchronizing signal which passed this gate circuit 22b, ID signal is detected by ID signal detector 48b from the signal acquired through a delay circuit 46, and a block number is detected by block number detector 52b. And a parity check is performed by parity check circuit 50b, and ID signal is checked for no error.

[0052] Moreover, the block number detected from ID signal by block number detector 52b is given to a comparator circuit 104. Moreover, the value which the block number before 1 sink block outputted through switch 54b was latched by latch circuit 56b, and added "1" further by +1 adder 58b is given to a comparator 104. In a comparator 104, these two inputs are measured and it is judged for a block number whether it is the right.

[0053] Thus, in the processing relevant to the synchronizing signal which passed gate circuit 22b, while the parity check of ID signal is performed, the check of a block number is also performed, when these both are O.K., as for switches 54b and 106, the output from block number detector 52b is chosen, both the terminal of that bottom, i.e., switch 54b, and a switch 106 chooses the synchronizing signal outputted from gate circuit 22b. And when either is NG at least among the result of ID parity check in parity check circuit 50b, and the detection result in block number detector 52b when other namely, in switches 54b and 106, an upper terminal, i.e., switch 54b, chooses the output of switch 54a, respectively, and a switch 106 chooses the output of delay circuit 108a.

[0054] In addition, delay circuits 102b, 108a, and 108b are for adjusting the time lag which follows a circuit system on passing a signal. And it is used as a row address of the memory for error corrections in the error correction circuit 64, the output, i.e., the block number, of switch 54b, and the output of a switch 106 is inputted into a pulse generator 110, and the output from a pulse generator 110 is used as a reference signal of the serial/parallel-conversion machine 66 and the column address counter 65.
[0055] Thus, although it is stored in the memory for error corrections in the error correction circuit 64 after serial/parallel conversion of the signal outputted from the delay circuit 46 is carried out in the serial/parallel-conversion circuit 66, at this time, the output of the column address counter 65 determines the column address of the memory for error corrections in the error correction circuit 64, and the block number outputted from switch 54b determines the row address of the memory for error corrections in the error correction circuit 64.
[0056] Such synchronizing signal detection actuation of a magnetic recorder and reproducing device 100 will become still clearer if drawing 11 is referred to. That is, drawing 11 (A) shows the output wave of the synchronizing signal detector 18, O in drawing shows a right synchronizing signal, and x shows an error synchronizing signal. That is, in this drawing, it is assumed that the 6th synchronizing signal (Sync6) is an error synchronizing signal.
[0057] Drawing 11 (B) shows the gate signal of width of face a, i.e., the output of gate signal creation circuit 20a, on the basis of the synchronizing signal with which it was applied, the output signal of the synchronizing signal protection network 36, i.e., the protection, shown in drawing 11 (E), within gate signal creation circuit 20a, a counter etc. is used for this gate signal and it is created. There is no gate signal of width of face a near a synchronizing signal (Sync5), because the counter in gate signal creation circuit 20a is reset by the synchronizing signal which the gate was opened by the gate opening signal (drawing 11 (D)) outputted from the synchronous omission count circuit 40, and was detected by this just before a gate signal was created. In addition, in this example, if the condition that there is no synchronizing signal continues twice in the gate signal of width of face a, gate circuit 22a will be opened compulsorily, and if the following synchronizing signal is detected in that condition, the case where the gate closes again is shown.
[0058] Here, the synchronizing signal (obtained from a protection synchronizing signal) which attached x although the synchronizing signal (Sync2) and synchronizing signal (Sync3) which are shown in drawing 11 are a right synchronizing signal, as a mask carried out with a gate signal, and detected as an error synchronizing signal, instead shown in drawing 11 (E) only in for example, gate circuit 22a will be detected accidentally.
[0059] Drawing 11 (C) shows the gate signal of gate width b, i.e., the output signal of gate circuit 22b, and comes to show the synchronizing signal to which the gate was applied by this gate signal in drawing 1111 (F). In this drawing 11 (F), since it is shown that the synchronizing signal which attached O is a right synchronizing signal, and the result of parity check circuit 50b serves as O.K., and the comparison result of a comparator circuit 104 is also in agreement, the switch 106 shown in drawing 10 switches to the bottom, and the synchronizing signal of drawing 11 R> 1 (F), i.e., drawing 11 , (J) is chosen.
[0060] On the other hand, since the synchronizing signal which attached x by drawing 11 (F) is an error synchronizing signal, as shown in drawing 11 (G), the result of parity check circuit 50b serves as NG (low level), and as shown in drawing 11 (H), the comparison result of a comparator circuit 104 serves as an inequality (low level). At this time, a switch 106 switches to the bottom and the synchronizing signal of drawing 11 (E) (I), i.e., drawing 9 , is outputted. Thus, the synchronizing signal outputted from a switch 106 comes to be shown in drawing 11 (K), and a right synchronizing signal without an error is detected.
[0061] Actuation of such a magnetic recorder and reproducing device is explained with reference to drawing 12 R> 2 and drawing 13 . As are shown in drawing 12 , and what gave "a" to the step number shows the processing about gate signal a and shows it to drawing 13 , what gave "b" to the step number shows the processing about gate signal b. Although these processings are performed by being parallel, processing of explanation concerning gate signal a first for convenience is explained previously.
[0062] First, in step S41a, if RS switching pulse is inputted, the gate of gate circuit 22a will be opened by gate signal creation circuit 20a in step S43a. On the other hand, after inputting "NO, i.e., RF switching pulse,", when step S41a is, Gate a is created by gate signal creation circuit 20a in step S45a. It progresses to step S47a after processing of step S43a and S45a.
[0063] In step S47a, detection of a synchronizing signal is performed by the synchronizing signal detector 18,

and it progresses to step S49a by it. In step S49a, if a synchronizing signal is not detected, it progresses to step S51a. In step S51a, if the gate opening signal is outputted from the synchronous omission count circuit 40, the gate of gate circuit 22a will be opened in step S53a, and it will return to step S47a. In step S51a, if the gate opening signal is not outputted, in step S55a, a protection synchronizing signal is created by protection synchronizing signal creation circuit 26a. When a synchronizing signal is detected by step S49a, it progresses to step S57a after processing of S55a, and ID signal is detected by ID signal detector 48a, and it progresses to step S59a. In step S59a, if ID parity check by gate signal b is O.K., it will progress to step S61a. If the value and the block number from block number detector 52b which added "1" to the sink block number before 1 sink block by gate signal b in step S61a are in agreement, it will connect with a lower terminal and switches 54b and 106 will progress to step S55b mentioned later.

[0064] When the time of step S59a being "NO" and step S61a are "NO(s)", it progresses to step S63a. In step S63a, if the parity check of ID signal is O.K. in parity check circuit 50a, in step S65a, a sink block number is loaded to the memory for error corrections in the error correction circuit 64. On the other hand, if step S63a is "NO", in step S67a, "1" is added to the block number in front of 1 synchronizing signal, and the value is stored in the memory for error corrections in step S69a.

[0065] On the other hand, in step S41b shown in drawing 13 , if RF switching pulse is given, the gate of gate circuit 22b will be opened in step S43b. If step S41b is "NO", in step S45b, gate signal b will be created by gate signal creation circuit 20b, and it will be given to gate circuit 22b. It progresses to step S47b after processing of step S43b and S45b.

[0066] In step S47b, if the gate opening signal by gate signal a is outputted, it will progress to step S49b. In step S49b, the gate of gate circuit 22b is opened and it progresses to step S51b. Also when step S47b is "NO", it progresses to step S51b. In step S51b, detection of a synchronizing signal is performed in the synchronizing signal detector 18, ID signal is detected by ID detector 48b in step S53b, and it progresses to step S55b.

[0067] In step S55b, if ID parity check in parity check circuit 50b is O.K., in step S57b, a sink block number will be detected by block number detector 52b, and it will progress to step S59b. In step S59b, if the value and the block number from block number detector 52b which added "1" to the block number before 1 sink block are in agreement, the sink block number is stored in the memory for error corrections in the error correction circuit 64 in step S61b.

[0068] When the time of step S55b being "NO" and step S59b are "NO(s)", it progresses to step S59a. In addition, step S61a is "YES", and when progressing to step S55b, naturally step S55b and S59b are set to "YES." Moreover, since step S55b and S59b are "NO(s)", when progressing to step S59a, naturally step S59a is set to "NO."

[0069] Furthermore, with reference to drawing 14 , the magnetic recorder and reproducing device 120 of other examples is explained. In addition, it becomes being the same as that of the magnetic recorder and reproducing device 10 which also shows circuit actuation to drawing 1 since it is fundamentally constituted similarly although gate width of the gate signal created in the gate signal creation circuit 20, corresponding to the detection result of the envelope detector circuit 42 like the magnetic recorder and reproducing device 10 which shows a magnetic recorder and reproducing device 120 to drawing 1 is not changed, and a switch 54 is usually controlled by the output of the parity check circuit 50 at the time of playback and mask actuation of a mask 122 is canceled. Therefore, the explanation which overlaps by attaching the same number is omitted.

[0070] Therefore, below, the main points which should be noted are explained among the actuation about the time of special playback. The sink block number outputted from a switch 54 is inputted into a comparator 124 and a latch circuit 126. The output of a latch circuit 126 is reset in the first transition of RF switching pulse, and the value has become "0" at the beginning. And the output of the parity check circuit 50 of ID signal is seen, and only when a parity check is O.K., the sink block number which is the output of a switch 54 is latched by the latch circuit 126.

[0071] That is, the output of a latch circuit 126 is updated only when the parity check of ID is O.K., and that whose parity check of ID is O.K. among sink block numbers smaller than the present sink block number is always outputted. This value is compared with a current sink block number, the write enable mask signal of a low level is outputted for a current sink block number from a comparator 124 at the time of below the sink block number from a latch circuit 126, the mask of the write enable signal is carried out in the mask circuit 122,

and the writing to the memory for error corrections in the error correction circuit 64 is stopped by the comparator 124. On the other hand, when the current sink block number is larger, a high-level write enable mask signal is outputted from a comparator 124, and data are written in on the address created with the sink block number and the KARAMO address counter 65.

[0072] Here, the mask circuit 122 is constituted as shown in drawing 1515 . The mask circuit 122 shown in drawing 2 contains OR circuit 128, the NOR gate 130, and an inverter 132. While the signal from an input terminal 61 is given to NOR circuit 130 through an inverter 132, the write enable mask signal from a comparator circuit 124 is given. The write enable signal from the output and input terminal 62 of NOR circuit 130 is given to OR circuit 128, and the output of OR circuit 128 is given to the error correction circuit 64 as an output of the mask circuit 122.

[0073] In the mask circuit 122, if the special regenerative signal and the write enable mask signal of a low level are outputted, a write enable signal will not be outputted to the error correction circuit 64. On the other hand, when the high-level write enable mask signal is outputted, a write enable signal is given to the error correction circuit 64. If it explains with reference to drawing 16 , from the synchronizing signal protection network 36, a protection synchronizing signal as shown in drawing 16 (A) will be outputted, and ID detection pulse as shown in drawing 16 (B) will be outputted from a pulse generator 44 according to it. And from the parity check circuit 50, a signal as shown in drawing 16 (C) is outputted. Since the protection synchronizing signal (Sync2) shown in drawing 16 (A) is mistaken, according to it, the output from the parity check circuit 50 is set to a low level.

[0074] As the sink block number outputted through a switch 54 shows drawing 16 (D) at this time, when the case where it is set to "30->25->32->33->34" is assumed, "25" is the mistaken sink block number. According to it, the sink block number from a latch circuit 126 is set to "29->30->30->32->33." "30" which the latch circuit 126 did not hold the mistaken sink block number "25", but incorporated it before that is held as it is so that drawing 16 (D) and (E) may be compared and understood. And a comparator 124 compares two signals inputted, and in below the sink block number from the latch circuit 126 which the present sink block number shown in drawing 16 (D) shows to drawing 16 (E), as shown in drawing 16 (F), a comparator 124 outputs the write enable mask signal of a low level in the mask circuit 122. Then, from OR circuit 128 of the mask circuit 122, a write enable signal is not outputted but the writing of the data to the memory for error corrections in the error correction circuit 64 is stopped.

[0075] Main actuation of such a magnetic recorder and reproducing device 120 is explained with reference to drawing 17 . First, in step S71 shown in drawing 17 , if RF switching pulse is given, it will progress to step S73. The gate of a gate circuit 22 is opened in step S73. On the other hand, if step S71 is "NO", in step S75, the gate signal of predetermined width of face will be created, and the gate will be set up. After processing of steps S73 and S75 progresses to step S77, respectively. In step S77, if detection of a synchronizing signal is performed and a synchronizing signal is not detected in step S79 in the synchronizing signal detector 18, it progresses to step S81. In step S81, if the gate opening signal is outputted from the synchronous omission count circuit 40, the gate of a gate circuit 22 will be opened in step S83, and it will return to step S77. On the other hand, if the gate opening signal is not outputted in step S81, in step S85, a protection synchronizing signal is created in the protection synchronizing signal creation circuit 38, and it progresses to step S87. Also when step S79 is "NO", it progresses to step S87.

[0076] In step S87, ID signal is detected in the ID detector 48, and if ID parity check is O.K. in step S89a in the parity check circuit 50, in step S91a, a sink block number will be latched by the latch circuit 126, and it will progress to step S93. It progresses to the direct step S93, without updating a sink block number, if the parity check of ID signal is NG in step S89a. Moreover, in after [processing] step S89b of step S87, a sink block number current in the block number detector 52 is detected, and it progresses to step S93.

[0077] In step S93, a sink block number current by the comparator 124 is compared with the sink block number from a latch circuit 126. If the current sink block number is larger, in step S95, a current sink block number will be written in the memory for error corrections in the error correction circuit 64. In step S93, if a current sink block number is below a sink block number from a latch circuit 126, in step S97, the writing of the data to the memory for error corrections in the error correction circuit 64 will be stopped.

[0078] In addition, although the above-mentioned example explained the magnetic recorder and reproducing device which records digital data on a magnetic tape, it cannot be overemphasized that this invention is

applicable also to the record regenerative apparatus of an optical recording method.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the important section of the reversion system of the magnetic recorder and reproducing device which is one example of this invention.
[Drawing 2] It is the block diagram showing an example of a gate signal creation circuit.
[Drawing 3] It is a timing chart for explaining actuation of a gate signal creation circuit.
[Drawing 4] It is a timing chart for explaining main actuation of the drawing 1 example.
[Drawing 5] It is the circuit diagram showing an example of a gate circuit.
[Drawing 6] It is the illustration Fig. showing the memory image of the memory for error corrections.
[Drawing 7] It is the flow chart which shows main actuation of the drawing 1 example.
[Drawing 8] It is the block diagram showing an example of the control circuit which controls the width of face of the gate based on the lock condition of PLL.
[Drawing 9] (A) is the timing chart showing actuation of a control circuit when PLL locks, and (B) is the timing chart showing actuation of a control circuit when PLL does not lock.
[Drawing 10] It is the block diagram showing the important section of the reversion system of the magnetic recorder and reproducing device which are other examples of this invention.
[Drawing 11] It is a timing chart for explaining main actuation of the drawing 10 example.
[Drawing 12] It is the flow Fig. showing main actuation of the drawing 10 example.
[Drawing 13] It is the flow Fig. showing a continuation of actuation of drawing 12 .
[Drawing 14] It is the block diagram showing the important section of the reversion system of the magnetic recorder and reproducing device which is the example of others of this invention.
[Drawing 15] It is the circuit diagram showing an example of a mask circuit.
[Drawing 16] It is a timing chart for explaining main actuation of the drawing 14 example.
[Drawing 17] It is the flow Fig. showing main actuation of the drawing 14 example.
[Drawing 18] It is an illustration Fig. for explaining a record format of a digital video tape recorder.
[Drawing 19] It is an illustration Fig. for explaining the record condition of the signal of a digital video tape recorder.
[Drawing 20] It is the block diagram showing the detailed configuration of 1 sink block of the signal in a digital video tape recorder.
[Drawing 21] It is an illustration Fig. for explaining the protected operation of a synchronizing signal.
[Drawing 22] It is the block diagram showing the conventional technique.
[Description of Notations]
10,100,120 -- Magnetic recorder and reproducing device
15 -- PLL Circuit
18 -- Synchronizing Signal Detector
20, 20a, 20b -- gate signal creation circuit
22, 22a, 22b, 60 -- Gate circuit
36 -- Synchronizing Signal Protection Network
38 -- Protection Synchronizing Signal Creation Circuit
40 -- Synchronous Omission Count Circuit

42 -- Envelope Detector
48, 48a, 48b -- ID detector
50, 50a, 50b -- Parity check circuit
52, 52a, 52b -- block number detector
54, 54a, 54b, 106 -- Switch
56, 56a, 56b, 126 -- Latch circuit
58, 58a, 58b --+1 adder
64 -- Error Correction Circuit
76 -- Control Circuit
104,124 -- Comparator
122 -- Mask Circuit

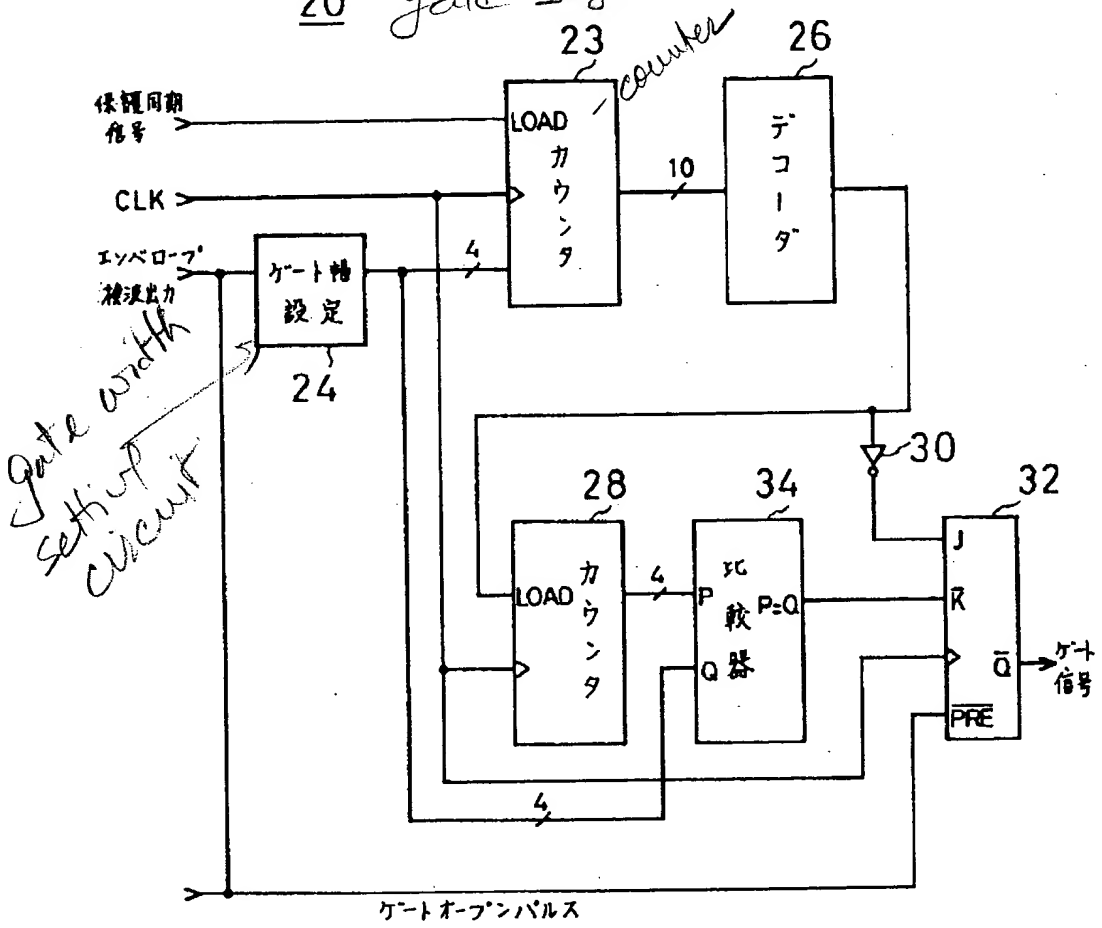
[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

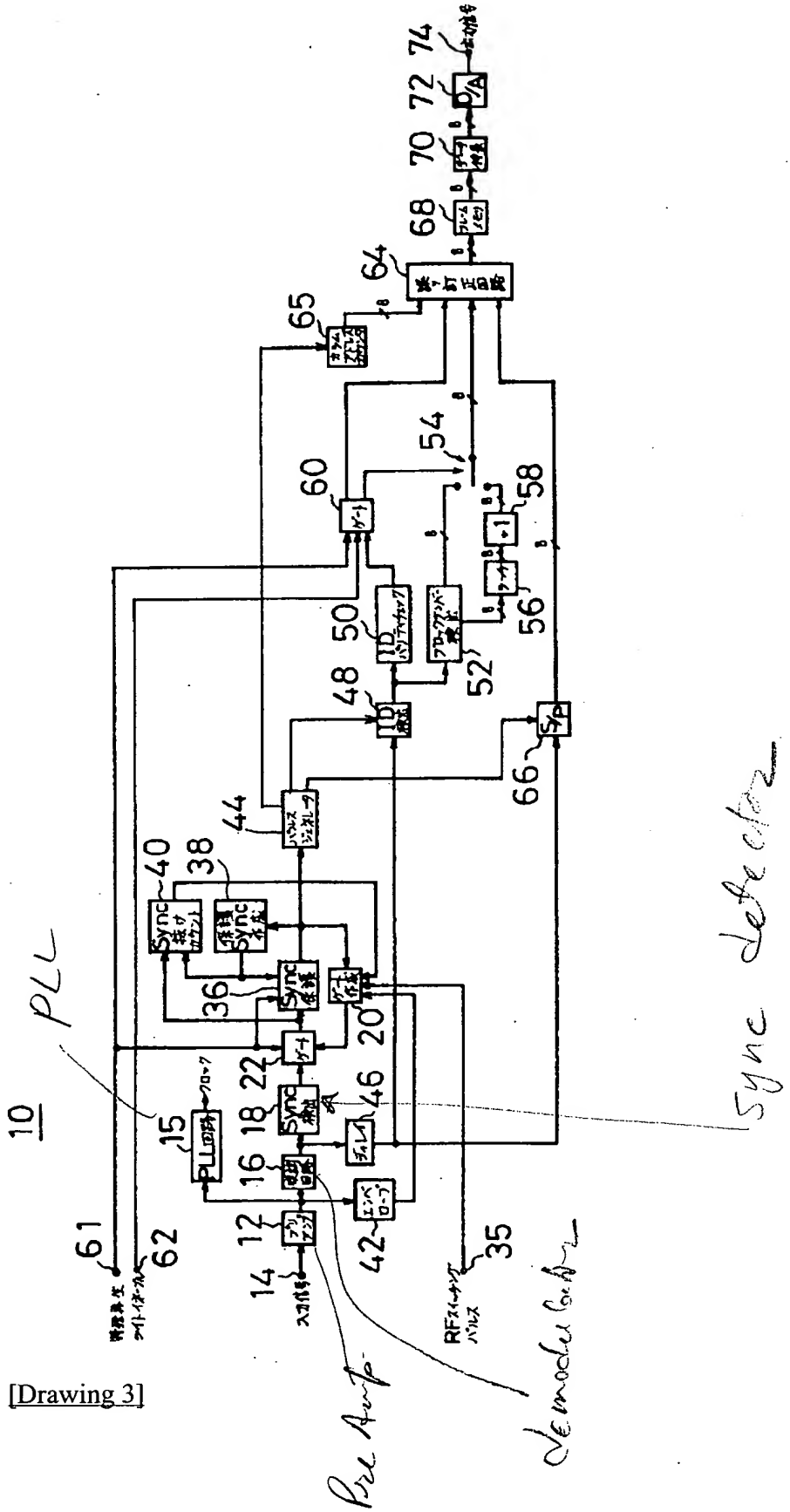
DRAWINGS

[Drawing 2]

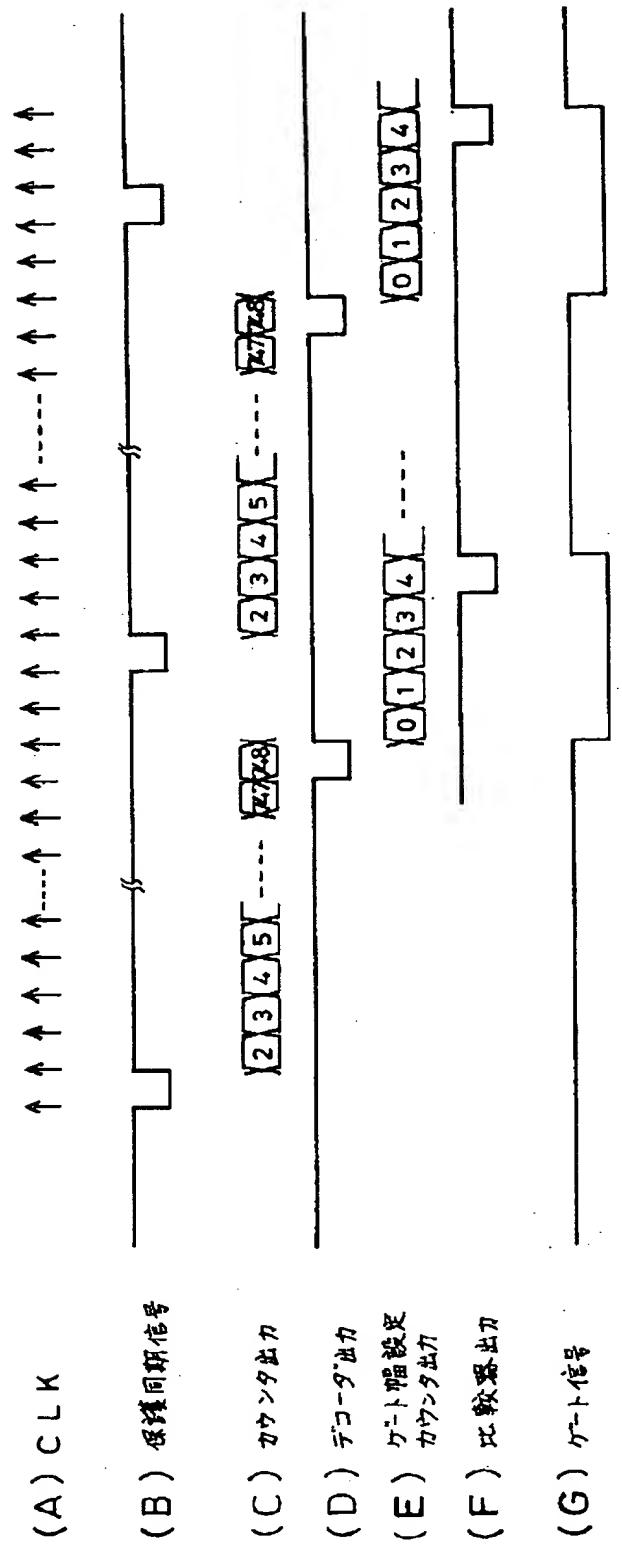


[Drawing 20]

[Drawing 1]



[Drawing 3]


(A) CLK
(B) 感磁同期信号
(C) カウンタ出力
(D) デコーダ出力
(E) ゲート幅設定 カウンタ出力
(F) 比較器出力
(G) ゲート信号
0 1 2 3 4
2 3 4 5

[Drawing 4]

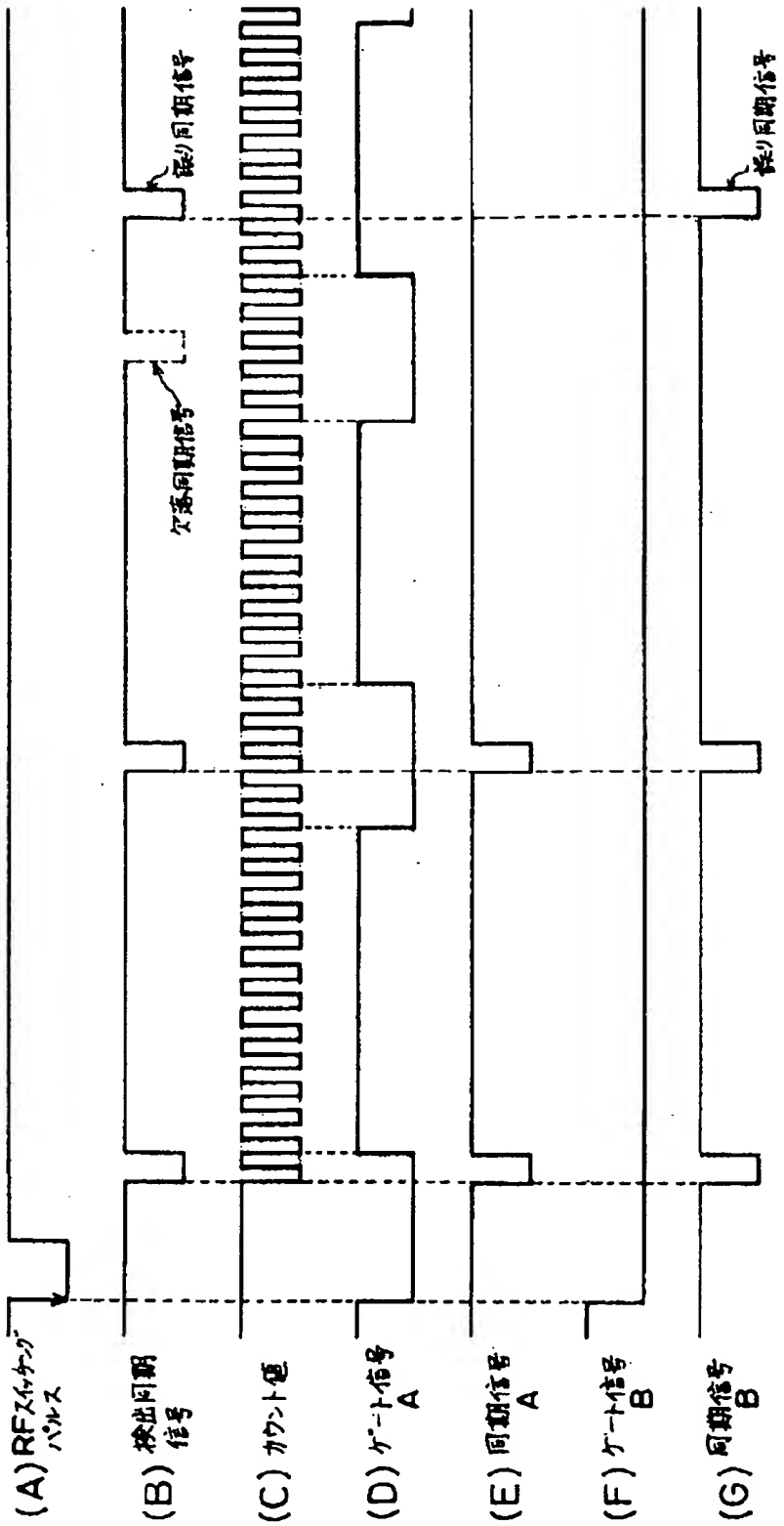
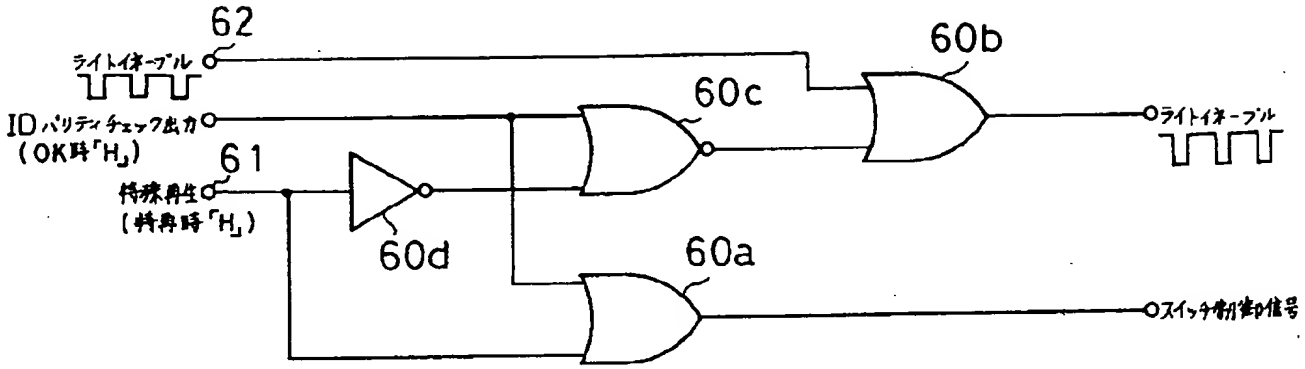


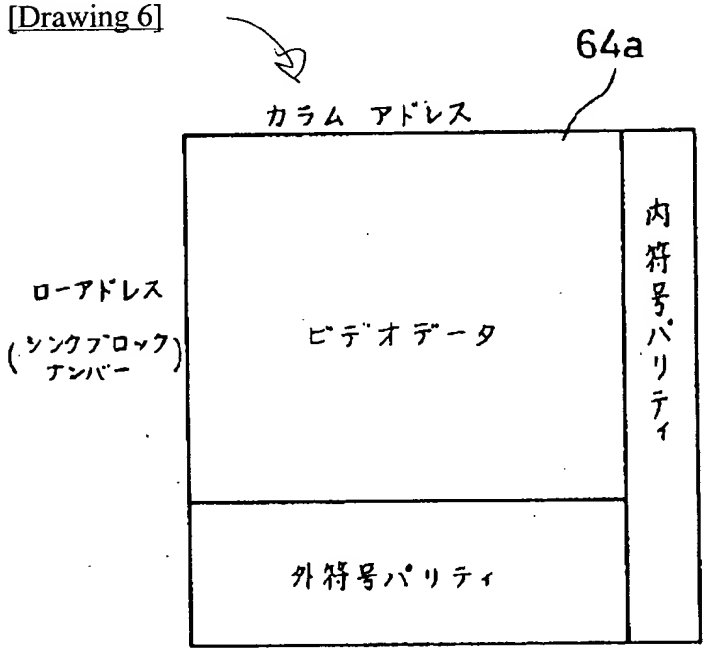
Fig. 4

[Drawing 5]

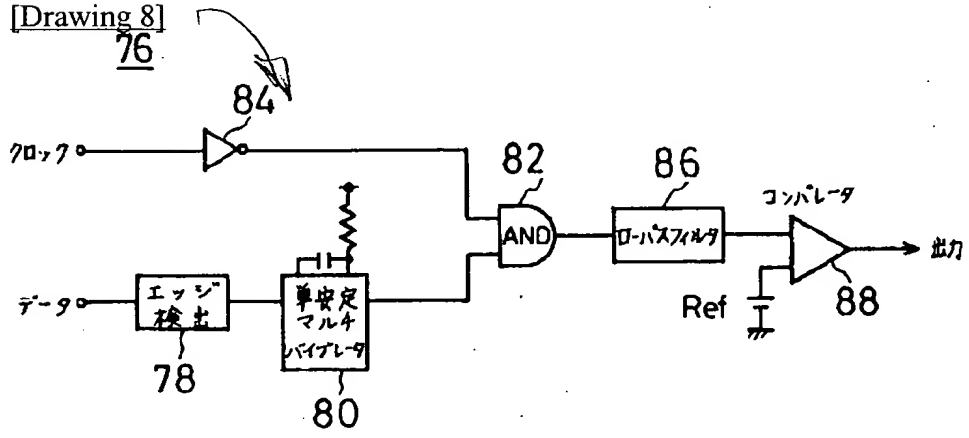
60



[Drawing 6]

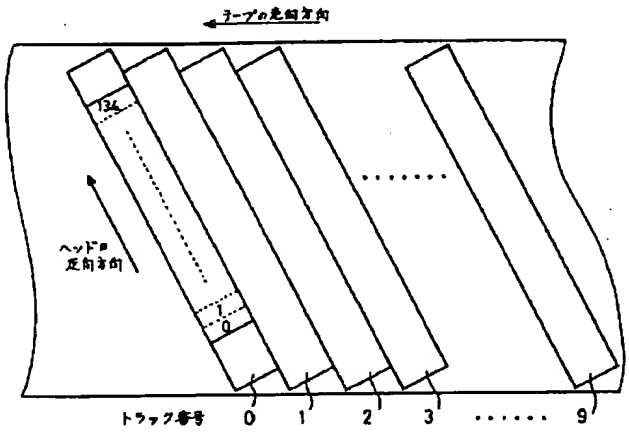


[Drawing 8]

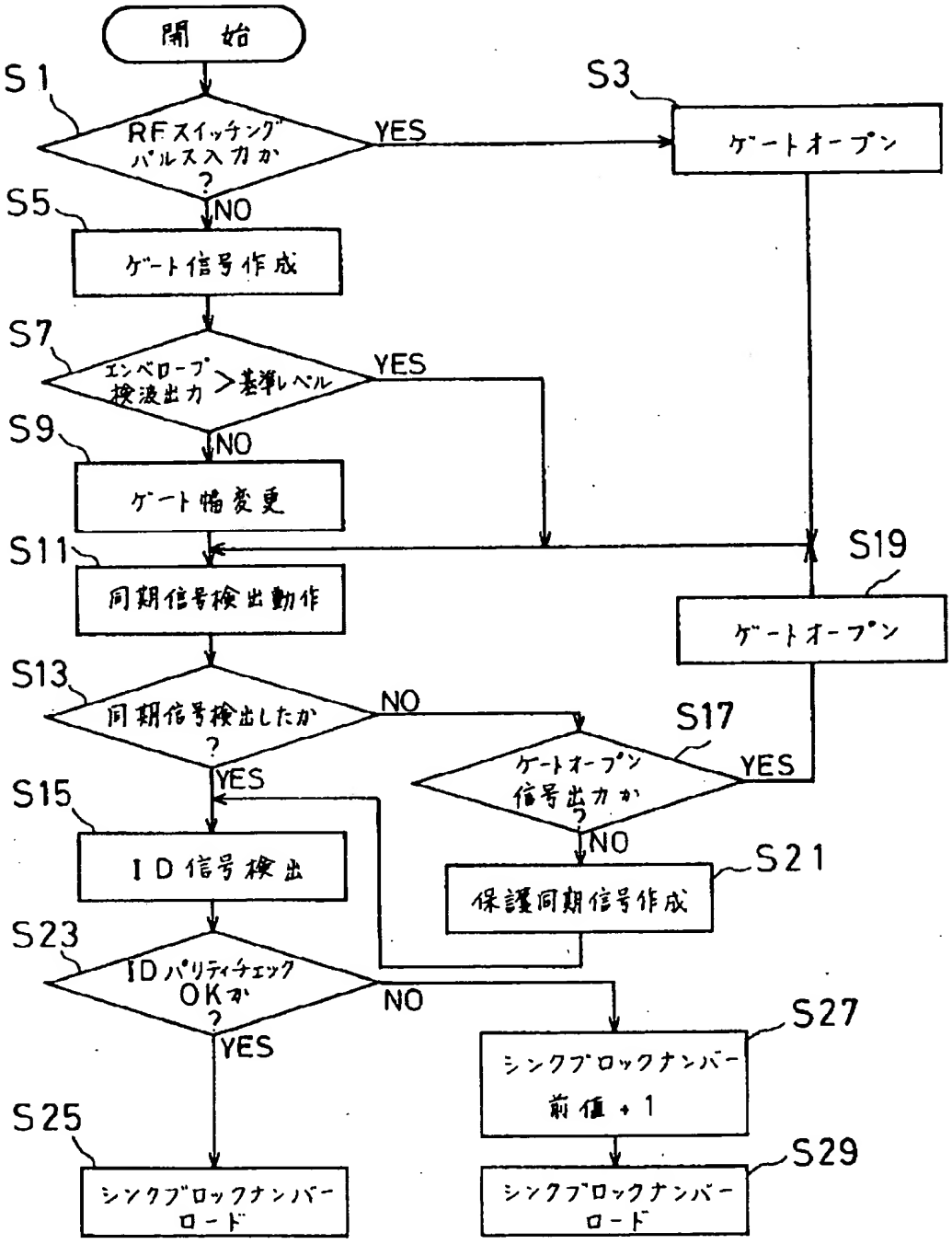


[Drawing 19]

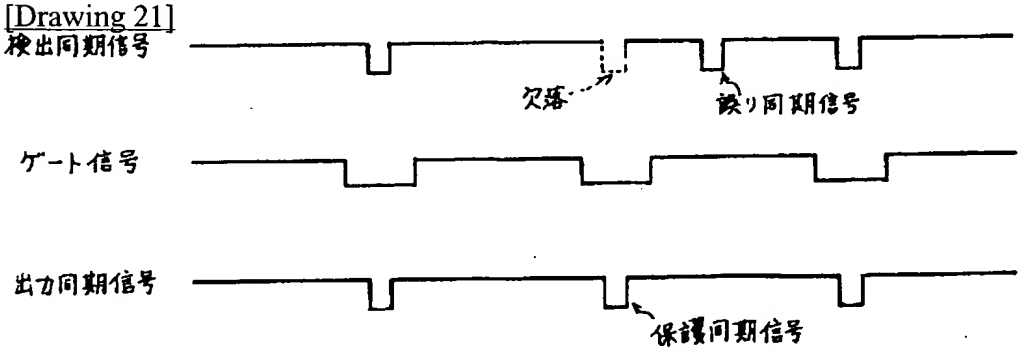
Dis 19



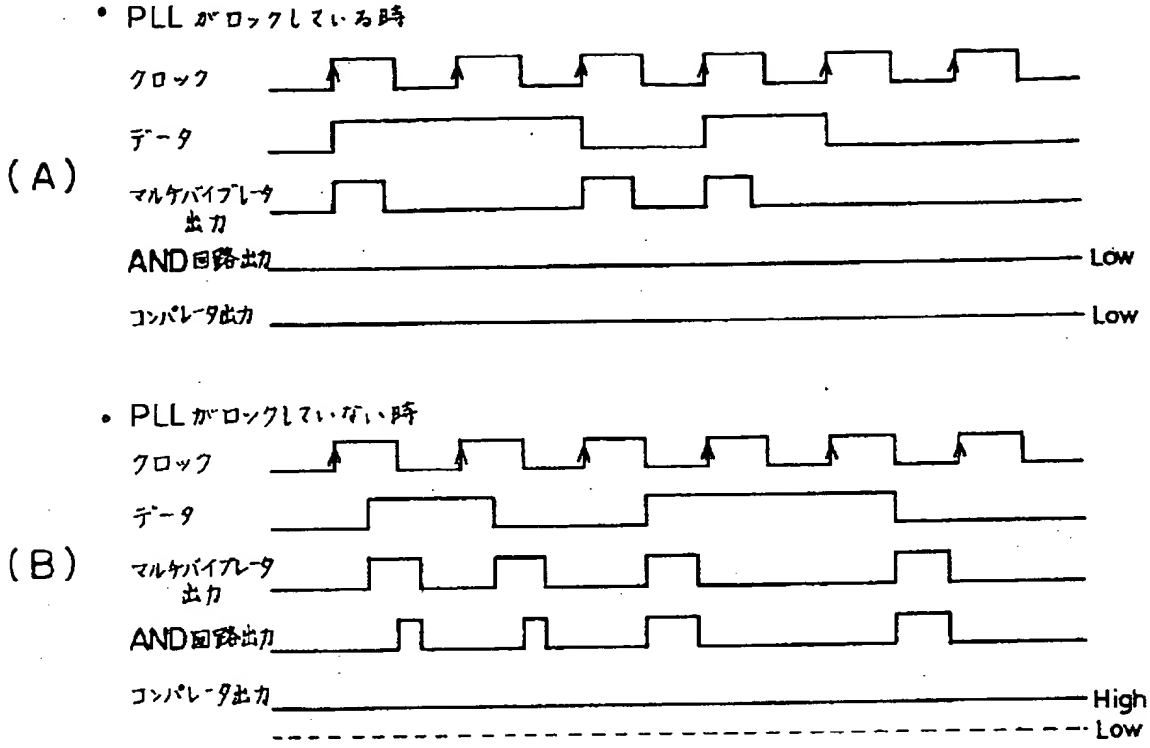
[Drawing 7]



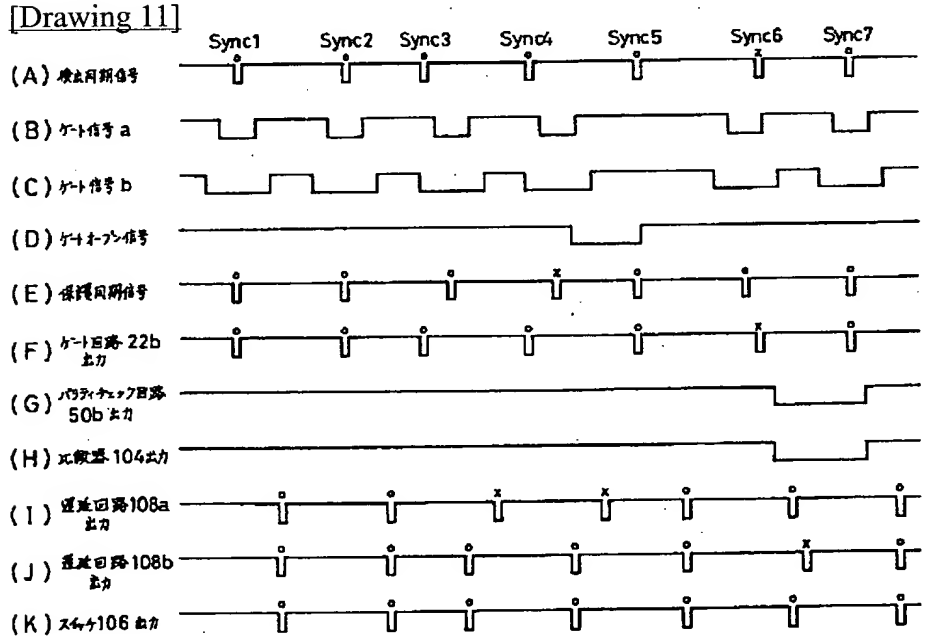
[Drawing 21]



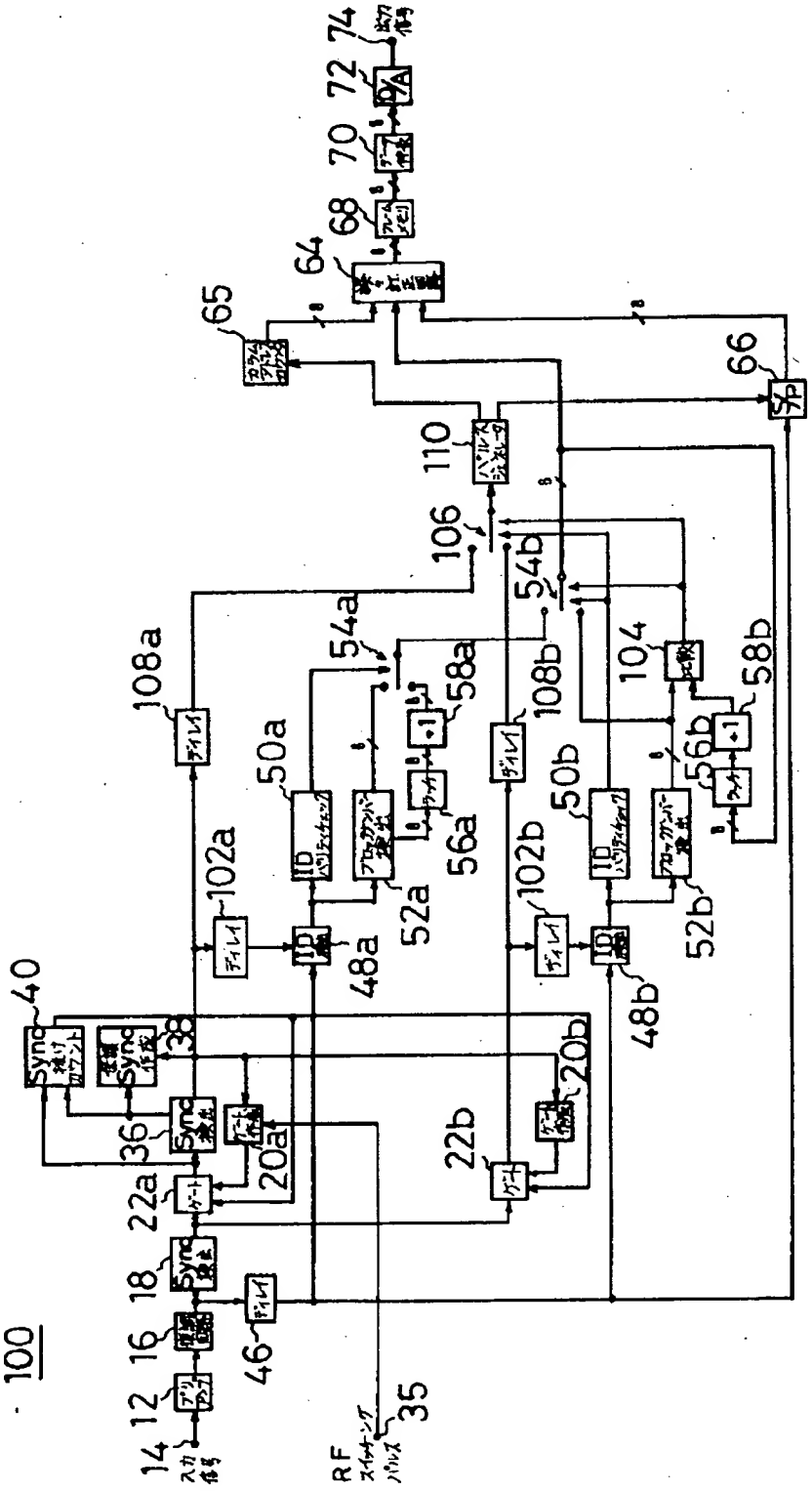
[Drawing 9]



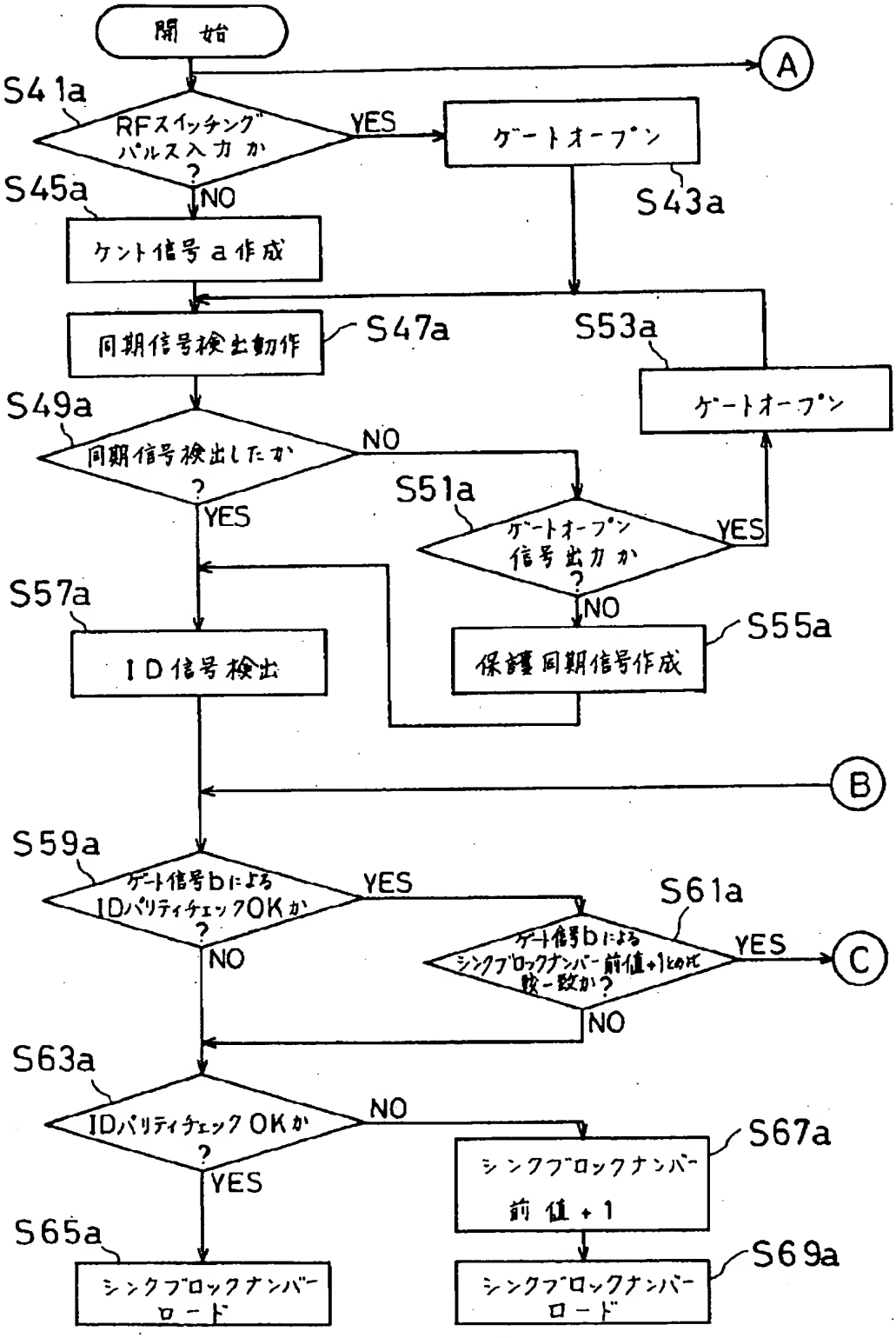
[Drawing 11]



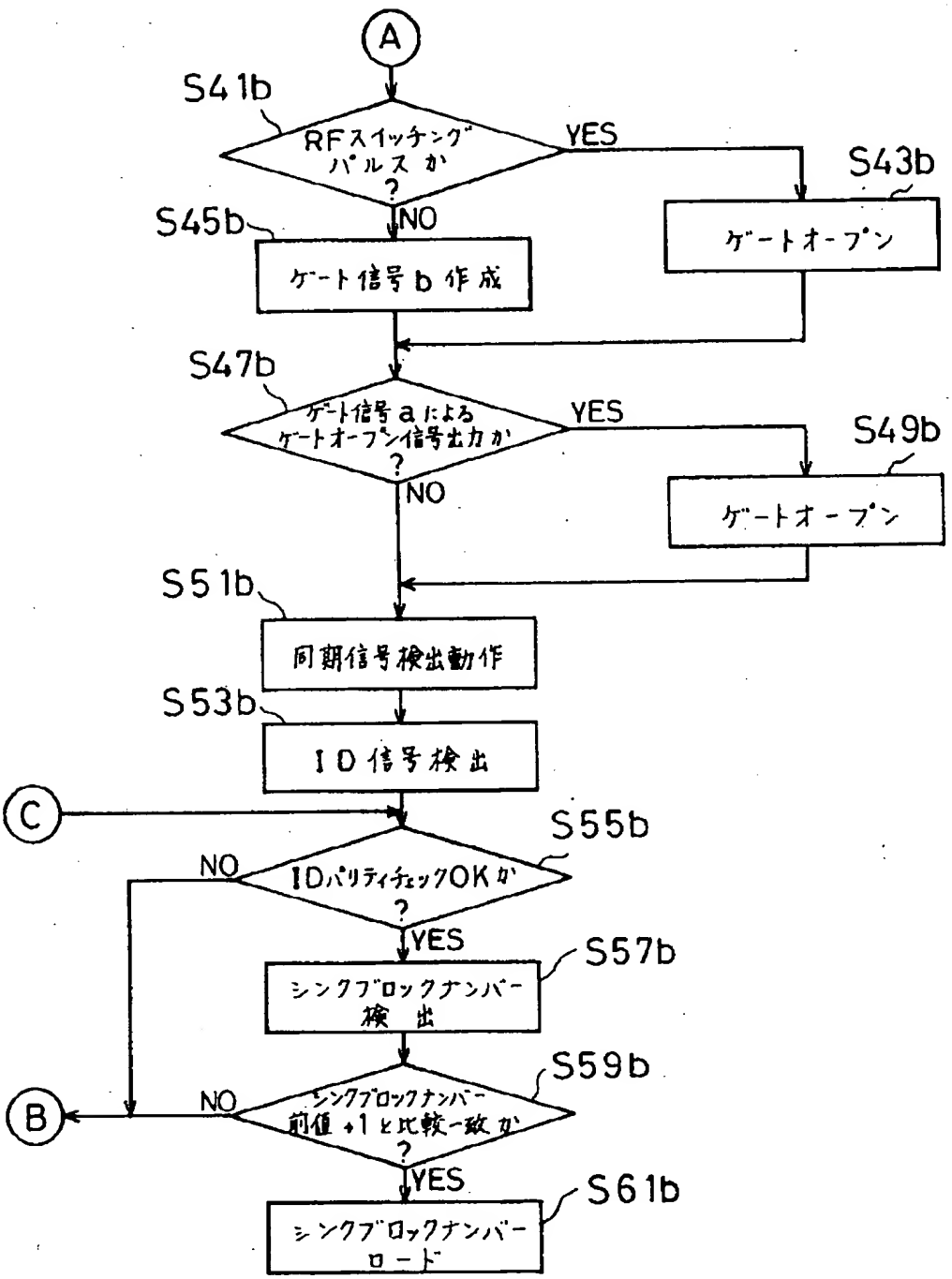
[Drawing 10]


100
40
38
36
18
16
12
14
46
35
RF
102a
102b
104
106
108a
108b
110
48a
48b
50a
50b
52a
52b
54a
54b
56a
56b
58a
58b
64
65
66
68
70
72
74
20a
20b
22a
22b

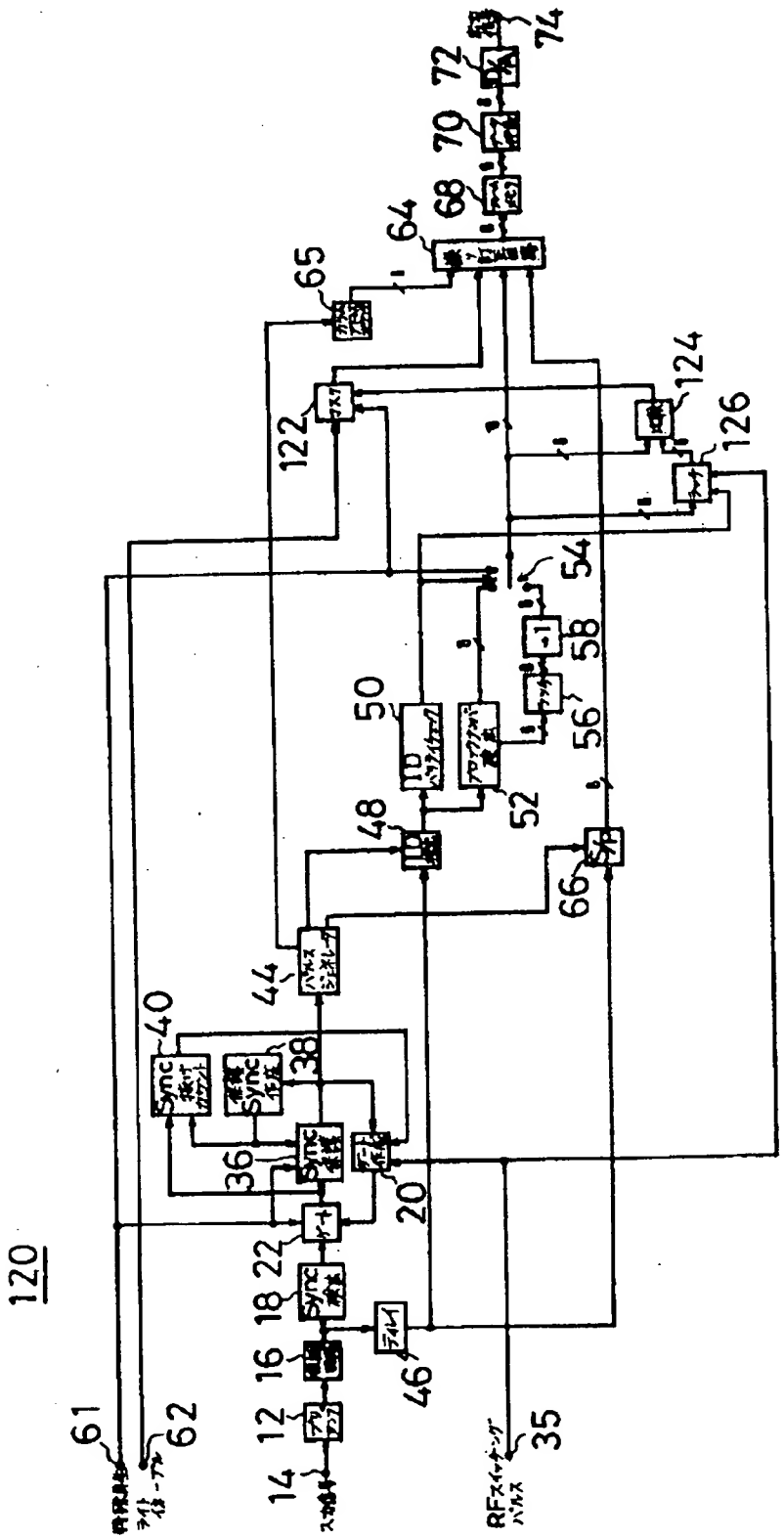
[Drawing 12]


開 始
A
S41a
RFスイッチング パルス入力か ?
YES
ゲートオープン
S43a
NO
S45a
ケント信号a作成
同期信号検出動作
S47a
S53a
ゲートオープン
S49a
同期信号検出したか ?
NO
YES
S51a
ゲートオープン 信号出力か ?
YES
NO
S57a
ID信号検出
保護同期信号作成
S55a
B
S59a
ゲート信号bによる IDパリティチェックOKか ?
YES
NO
S61a
ゲート信号bによる シンクブロックナンバー前値+1との 致一致か?
YES
C
NO
S63a
IDパリティチェックOKか ?
NO
YES
S67a
シンクブロックナンバー 前値+1
S65a
シンクブロックナンバー ロード
S69a
シンクブロックナンバー ロード

[Drawing 13]

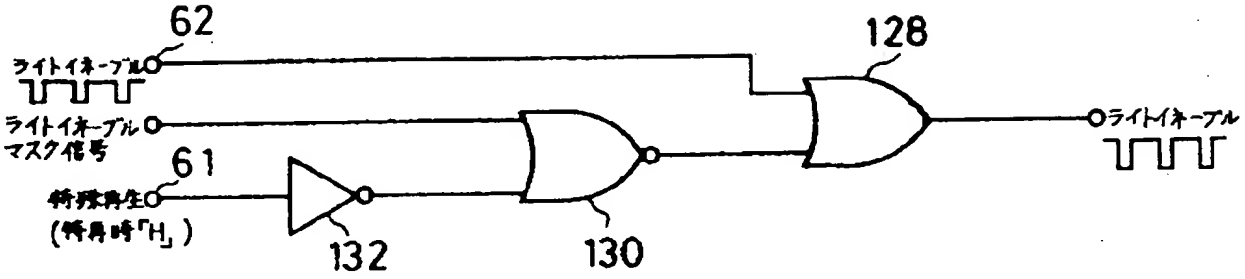

A
S41b
RFスイッチング パルス か ?
YES
NO
S43b
ゲートオープン
S45b
ゲート信号 b 作成
S47b
ゲート信号 a による ゲートオープン信号出力か ?
YES
NO
S49b
ゲートオープン
S51b
同期信号検出動作
S53b
ID 信号検出
C
S55b
NO
ID パリティチェック OK か ?
YES
S57b
シングブロックナンバー 検出
S59b
B
NO
シングブロックナンバー 前値 +1 と比較一致か ?
YES
S61b
シングブロックナンバー ロード

[Drawing 14]

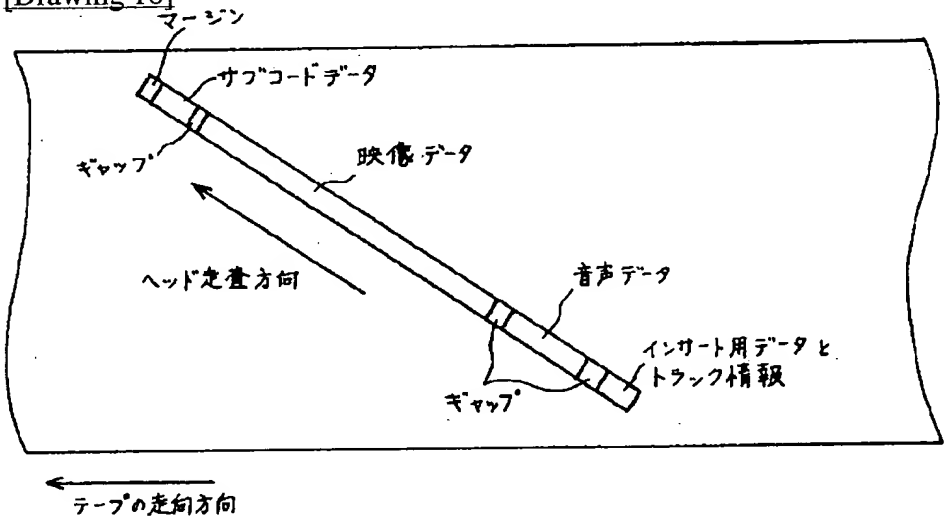

120
74
72
70
68
64
65
124
126
122
54
58
56
50
52
48
66
44
40
38
36
20
22
18
16
12
14
46
61
62
35

[Drawing 15]

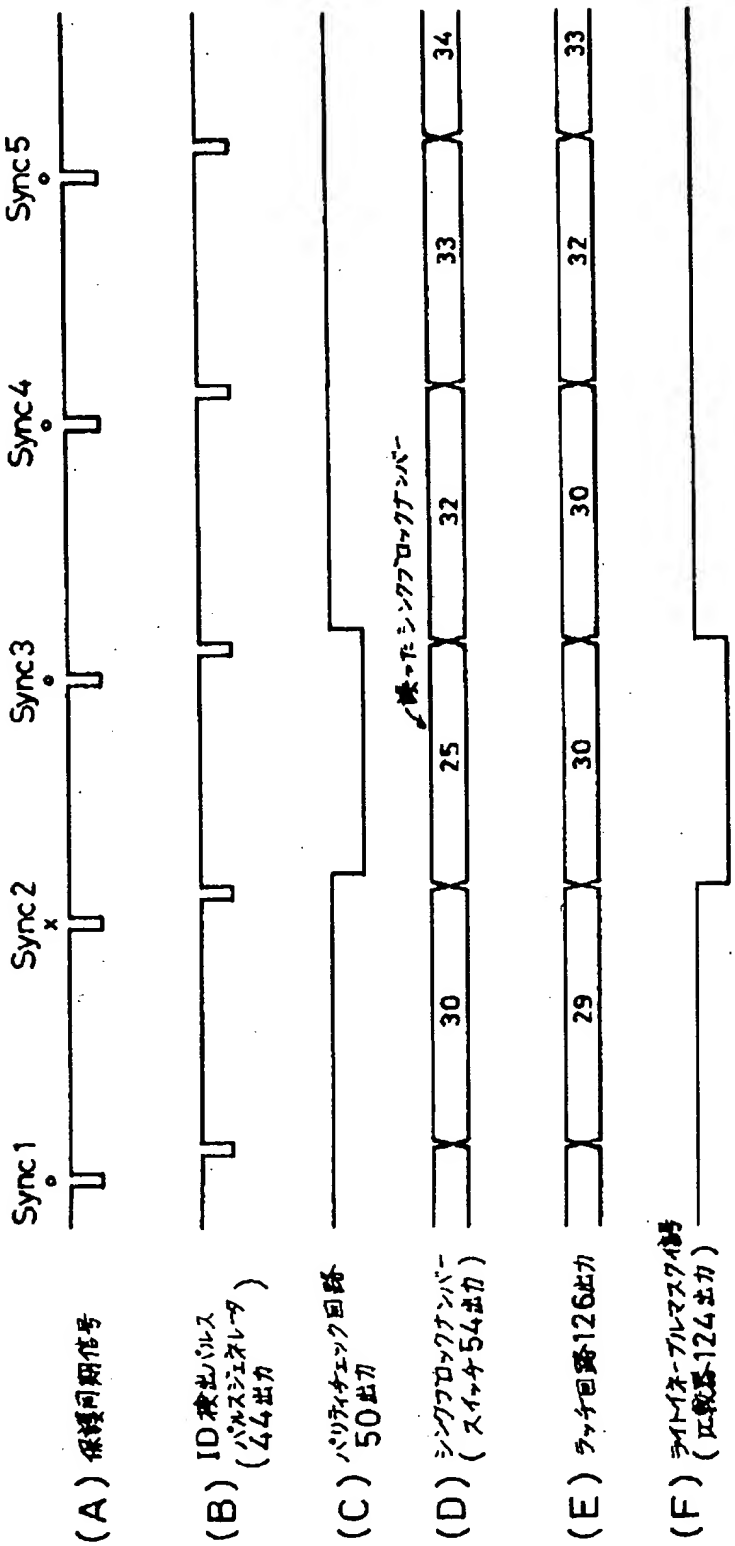
122



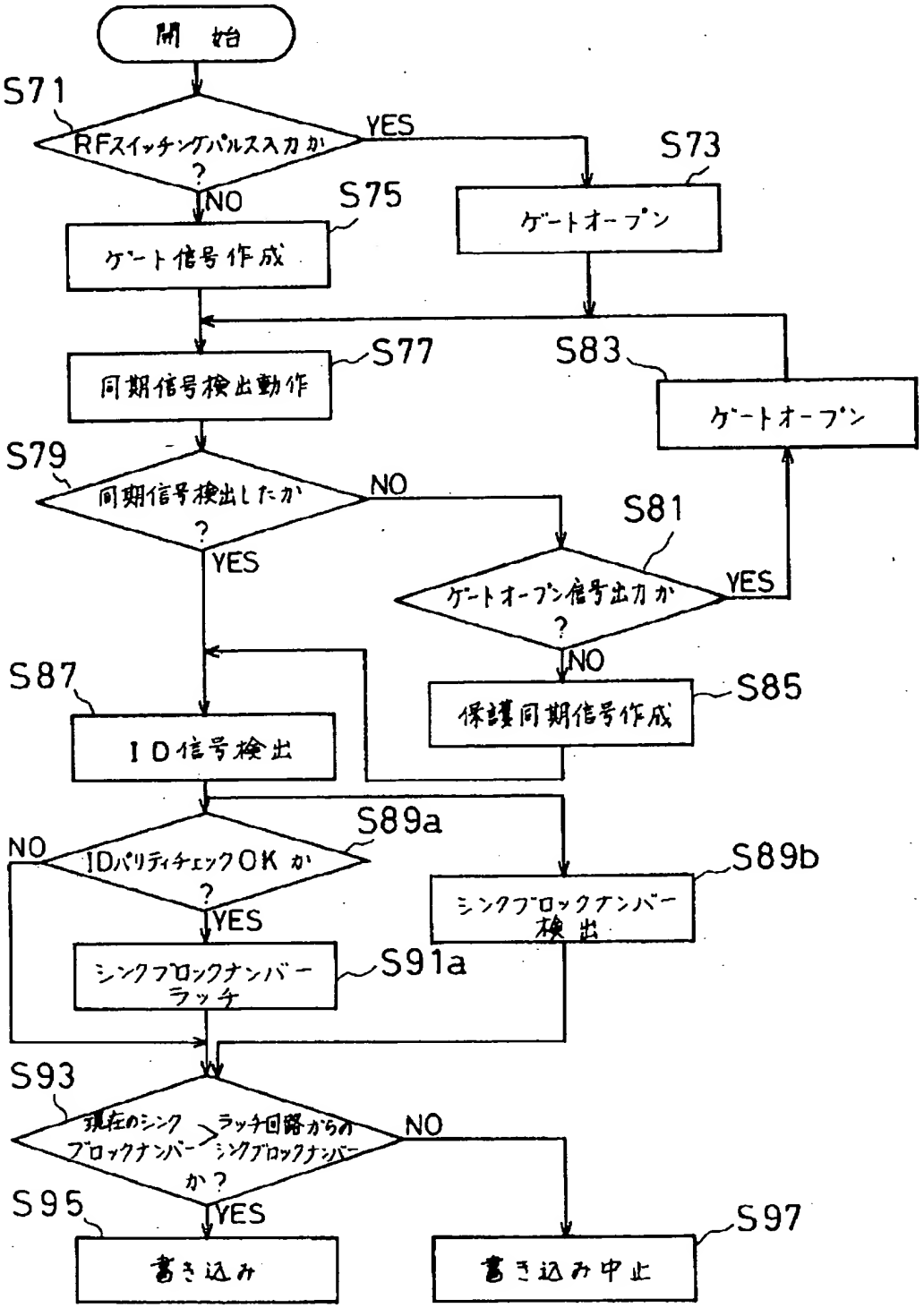
[Drawing 18]



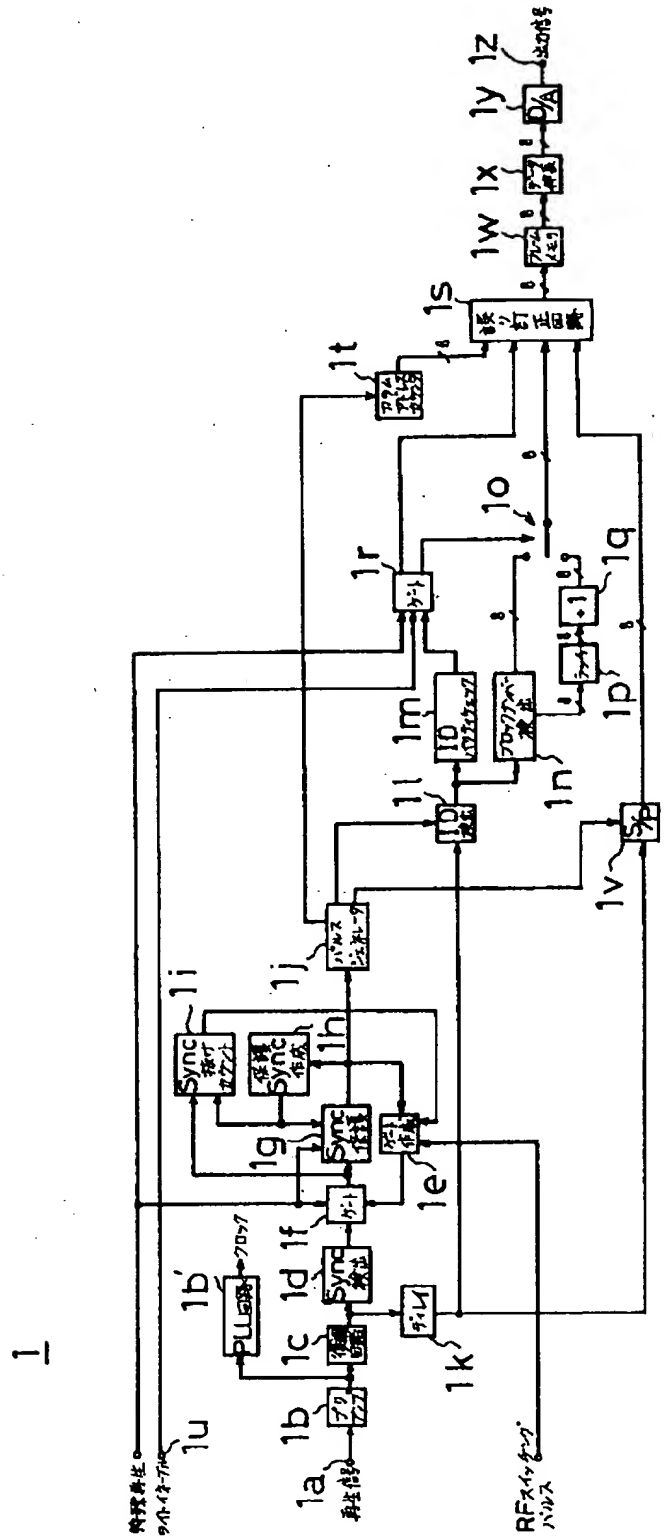
[Drawing 16]


Sync1
Sync2
Sync3
Sync4
Sync5
(A) 保護同期信号
(B) ID検出パルス (パルスジェネレータ44出力)
(C) パリティチェック回路 50出力
(D) シングロックナンバー (スイッチ54出力)
(E) ラッチ回路126出力
(F) ライトイネーブルマスク信号 (比較器124出力)
シングロックナンバー
30
25
32
33
34
29
30
30
32
33

[Drawing 17]


開 始
S71
RFスイッチングパルス入力か？
YES
NO
S73
ゲートオープン
S75
ゲート信号作成
S77
同期信号検出動作
S83
ゲートオープン
S79
同期信号検出したか？
NO
YES
S81
ゲートオープン信号出力か？
YES
NO
S87
ID信号検出
S85
保護同期信号作成
S89a
NO
IDパリティチェックOKか？
YES
S89b
シンクブロックナンバー検出
シンクブロックナンバーラッチ
S91a
S93
現在のシンクブロックナンバー＞ラッチ回路からのシンクブロックナンバーか？
NO
YES
S95
書き込み
S97
書き込み中止

[Drawing 22]



[Translation done.]